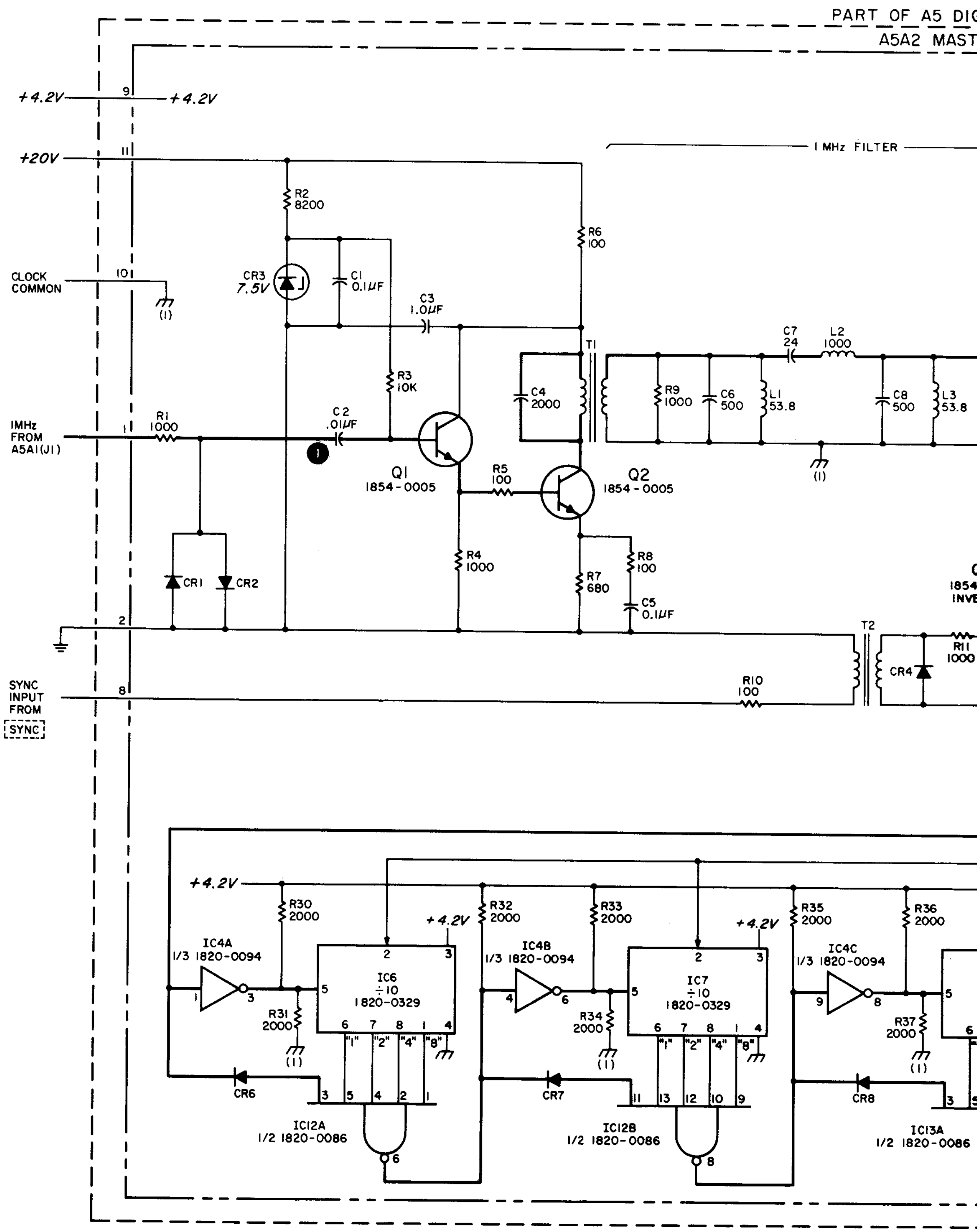
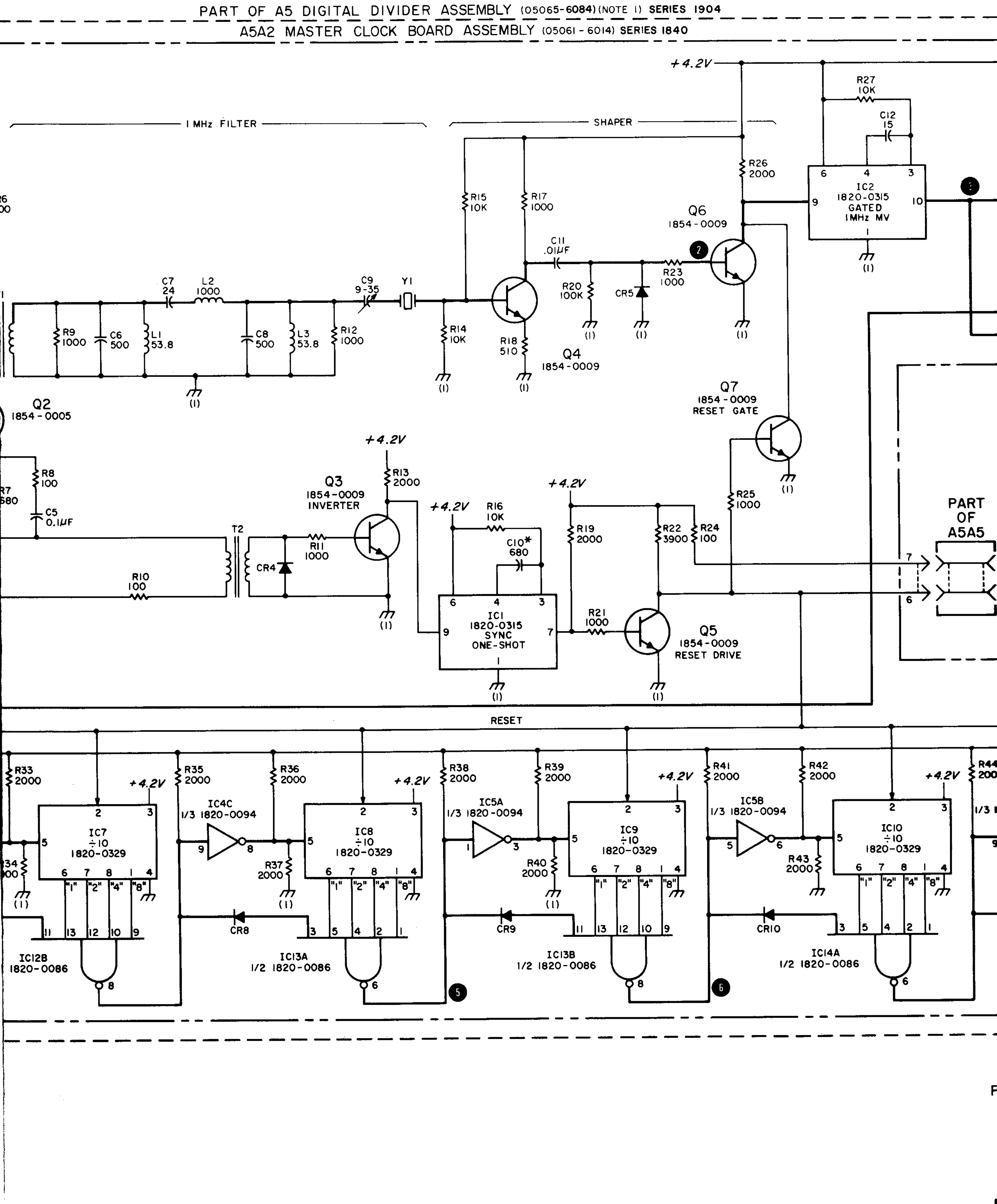


PART OF A5 DIG
A5A2 MAST
+4.2V
9
+4.2V
+20V
11
1 MHz FILTER
R2 8200
R6 100
CLOCK COMMON
10
(1)
CR3 7.5V
C1 0.1μF
C3 1.0μF
T1
C7 24
L2 1000
R3 10K
C4 2000
R9 1000
C6 500
L1 53.8
C8 500
L3 53.8
IMHz FROM A5A1(J1)
R1 1000
C2 .01μF
Q1 1854-0005
R5 100
Q2 1854-0005
R4 1000
R8 100
R7 680
C5 0.1μF
CR1
CR2
2
T2
R11 1000
CR4
SYNC INPUT FROM
SYNC
8
R10 100
+4.2V
R30 2000
IC4A 1/3 1820-0094
IC6 ÷10 1820-0329
R31 2000
CR6
IC12A 1/2 1820-0086
R32 2000
R33 2000
IC4B 1/3 1820-0094
IC7 ÷10 1820-0329
R34 2000
CR7
IC12B 1/2 1820-0086
R35 2000
R36 2000
IC4C 1/3 1820-0094
R37 2000
CR8
IC13A 1/2 1820-0086
"1" "2" "4" "8"



PART OF A5 DIGITAL DIVIDER ASSEMBLY (05065-6084) (NOTE 1) SERIES 1904
A5A2 MASTER CLOCK BOARD ASSEMBLY (05061-6014) SERIES 1840
1 MHz FILTER
SHAPER
+4.2V
R27 10K
C12 15
R26 2000
IC2 1820-0315 GATED 1MHz MV
Q6 1854-0009
R15 10K
R17 1000
C11 .01µF
R20 100K
CR5
R23 1000
C7 24
L2 1000
C9 9-35
Y1
R9 1000
C6 500
L1 53.8
C8 500
L3 53.8
R12 1000
R14 10K
R18 510
Q4 1854-0009
Q2 1854-0005
Q7 1854-0009 RESET GATE
R8 100
C5 0.1µF
Q3 1854-0009 INVERTER
R13 2000
R16 10K
C10* 680
R19 2000
R22 3900
R24 100
R25 1000
T2
R11 1000
CR4
R10 100
IC1 1820-0315 SYNC ONE-SHOT
R21 1000
Q5 1854-0009 RESET DRIVE
PART OF A5A5
RESET
R33 2000
R35 2000
R36 2000
R38 2000
R39 2000
R41 2000
R42 2000
IC7 ÷10 1820-0329
IC4C 1/3 1820-0094
IC8 ÷10 1820-0329
IC5A 1/3 1820-0094
IC9 ÷10 1820-0329
IC5B 1/3 1820-0094
IC10 ÷10 1820-0329
R37 2000
R40 2000
R43 2000
CR8
CR9
CR10
IC12B 1820-0086
IC13A 1/2 1820-0086
IC13B 1/2 1820-0086
IC14A 1/2 1820-0086

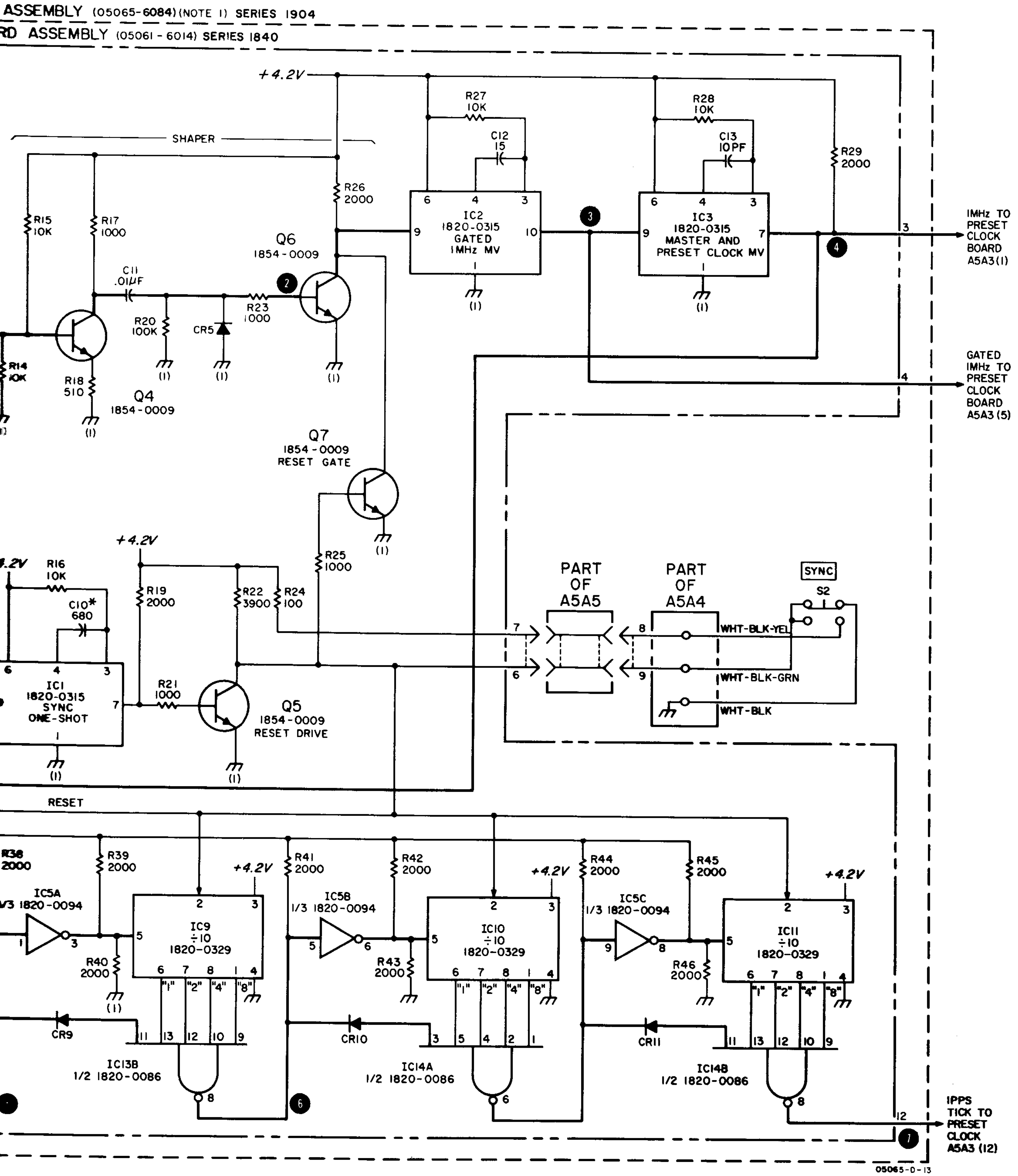
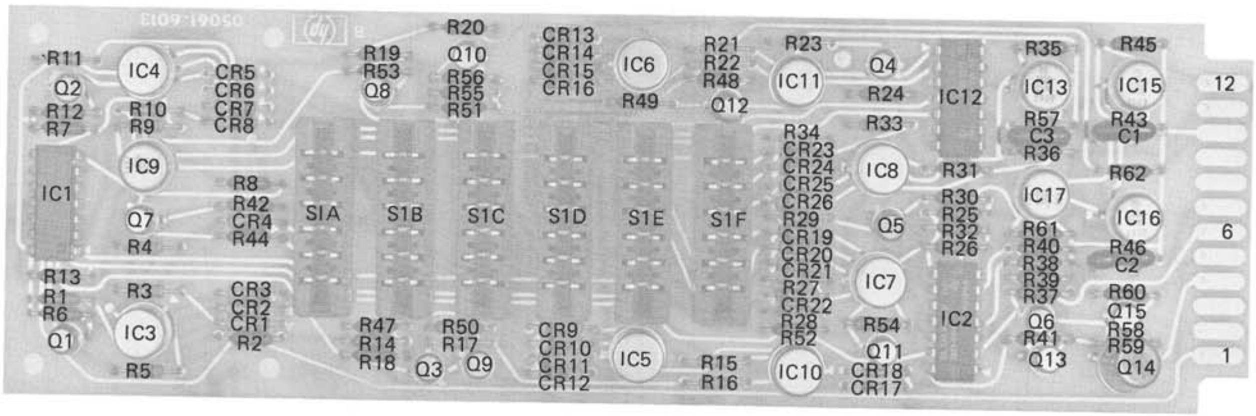
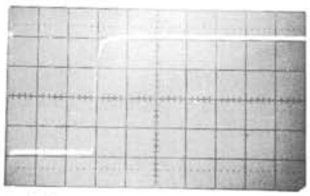
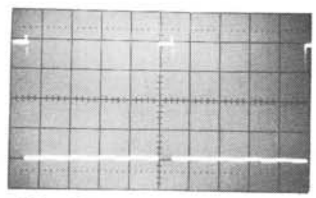
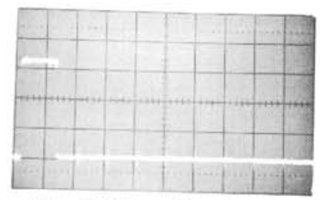


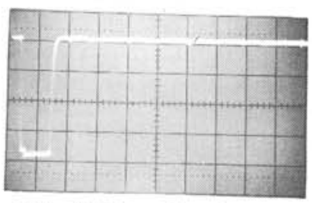
Figure 8-14. A5A2 Master Clock Board (Option 001)
(Sheet 2 of 3)

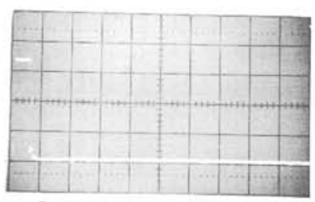


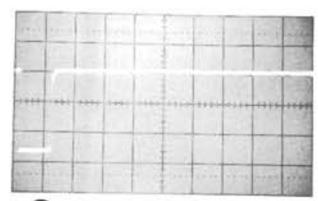

8 1 V/cm, 1 μs/cm

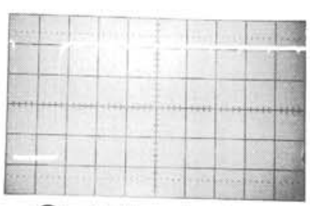

9 1 V/cm, 20μs/cm

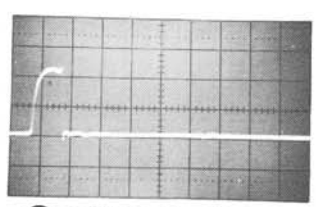

10 .5 V/cm, 1 μs/cm

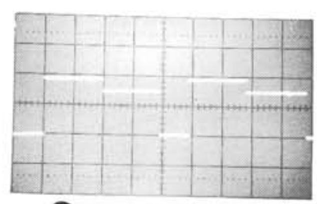

11 1 V/cm, .5 μs/cm

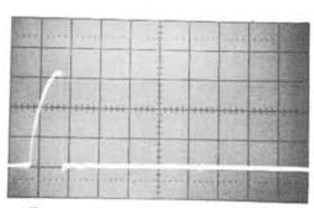

12 .5 V/cm, 2 μs/cm


13 1 V/cm, 1 μs/cm


14 1 V/cm, 1 μs/cm


15 1 V/cm, .2 μs/cm


16 1 V/cm, .2 μs/cm


17 1 V/cm, .2 μs/cm

5065A: Normal operation unless noted.

Oscilloscope: DC coupled

Figure 8-15
A5A3 PRESET CLOCK BOARD (OPTION 001)
(Sheet 3 of 3)

(See Page 8-37)

NOTES

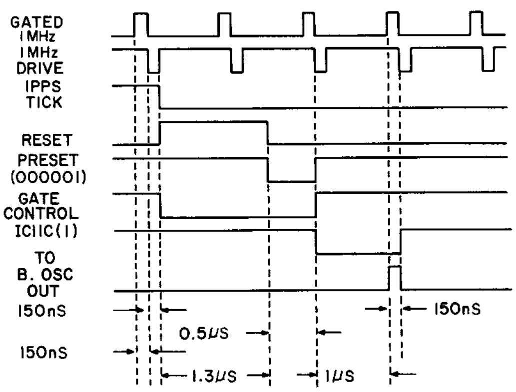
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

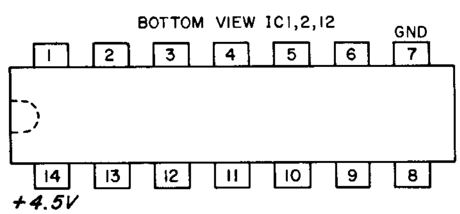
REFERENCE DESIGNATIONS

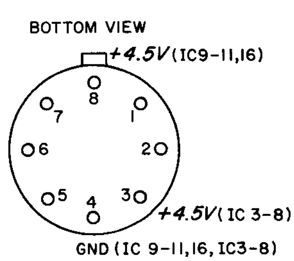
A5A3
C1-3 CR1-26 IC1-17 Q1-15 R1-62 S1

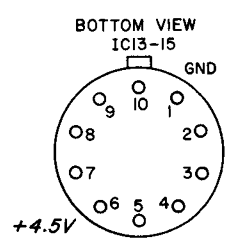
SWITCH LOGIC FOR PRESET SWITCHES S1 THRU S6

		PRESET SWITCH POSITION									
		0	1	2	3	4	5	6	7	8	9
COMMON (C) CONNECTED TO	1	▲		▲		▲		▲		▲	
	2			▲	▲			▲	▲		
	4			▲	▲	▲	▲				
	8	▲	▲								

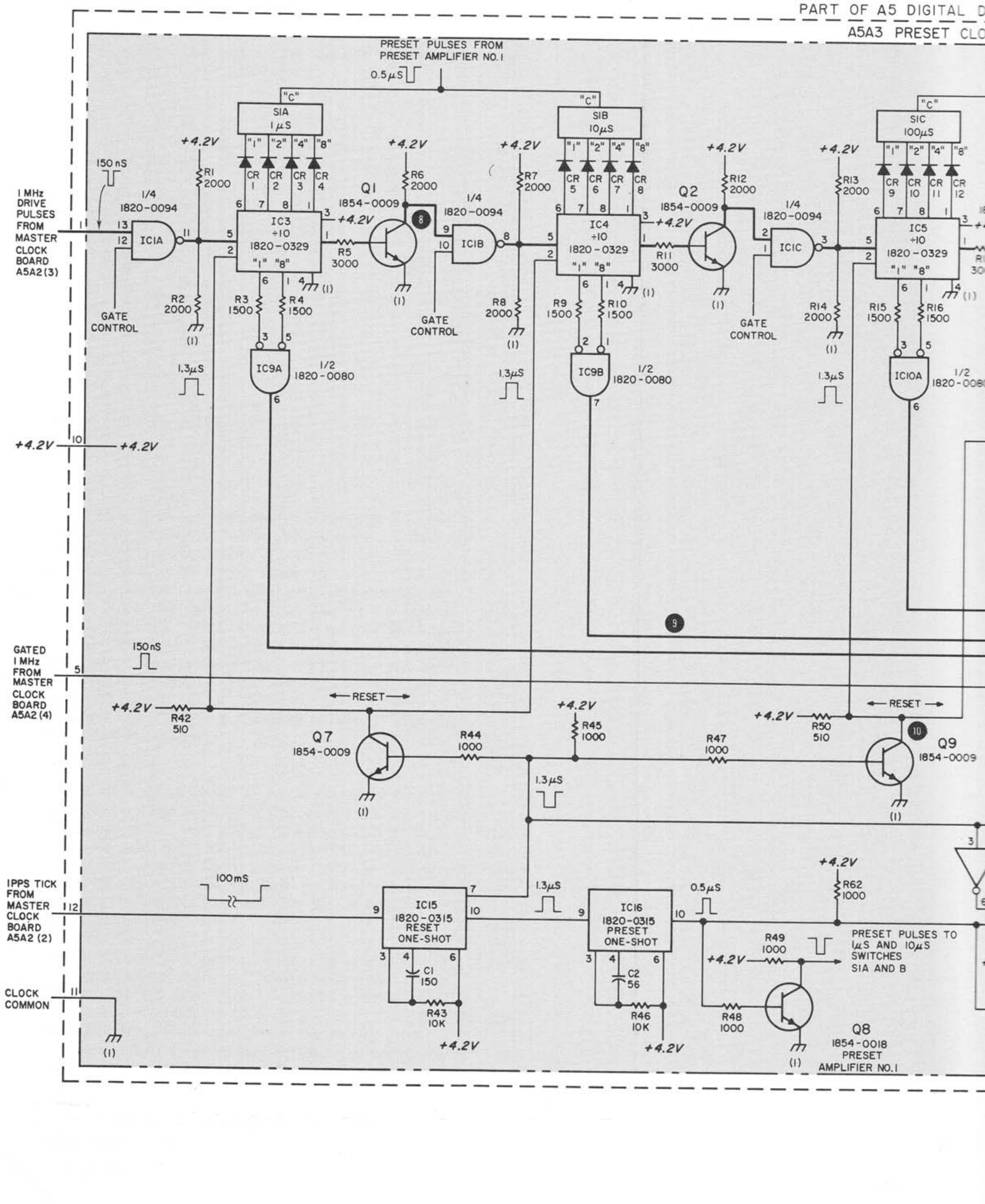


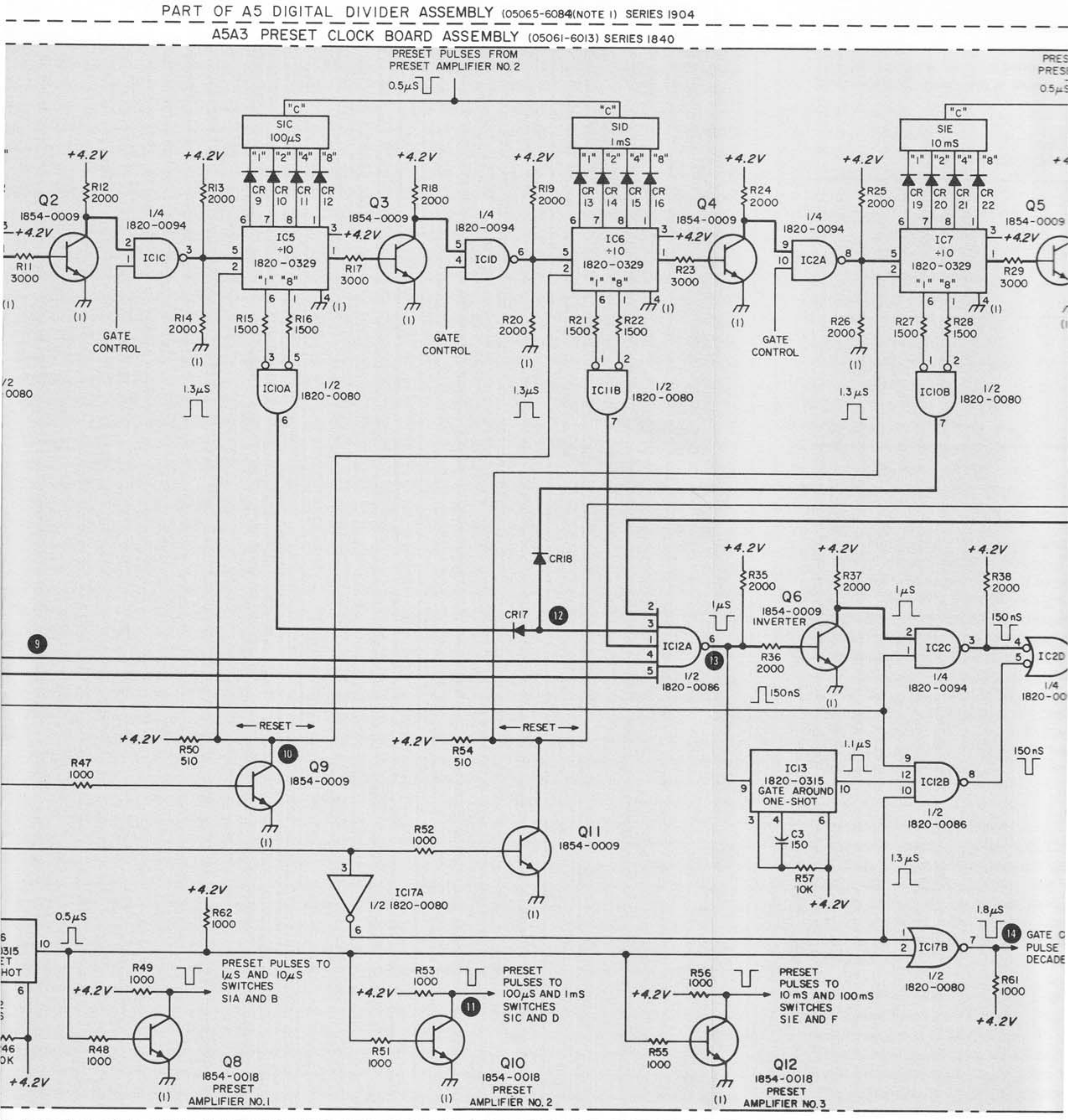






05065-D-14


PART OF A5 DIGITAL D
A5A3 PRESET CLO
PRESET PULSES FROM PRESET AMPLIFIER NO. 1
0.5μS
S1A 1μS
S1B 10μS
S1C 100μS
"C"
"1" "2" "4" "8"
CR 1 CR 2 CR 3 CR 4
CR 5 CR 6 CR 7 CR 8
CR 9 CR 10 CR 11 CR 12
+4.2V
R1 2000
R2 2000
R3 1500
R4 1500
R5 3000
R6 2000
R7 2000
R8 2000
R9 1500
R10 1500
R11 3000
R12 2000
R13 2000
R14 2000
R15 1500
R16 1500
150 nS
1 MHz DRIVE PULSES FROM MASTER CLOCK BOARD A5A2(3)
1/4 1820-0094
IC1A
IC1B
IC1C
IC3 ÷10 1820-0329
IC4 ÷10 1820-0329
IC5 ÷10 1820-0329
Q1 1854-0009
Q2 1854-0009
GATE CONTROL
IC9A 1/2 1820-0080
IC9B 1/2 1820-0080
IC10A 1/2 1820-0080
1.3μS
GATED 1 MHz FROM MASTER CLOCK BOARD A5A2 (4)
R42 510
RESET
Q7 1854-0009
R44 1000
R45 1000
R47 1000
R50 510
Q9 1854-0009
IPPS TICK FROM MASTER CLOCK BOARD A5A2 (2)
100 mS
IC15 1820-0315 RESET ONE-SHOT
C1 150
R43 10K
IC16 1820-0315 PRESET ONE-SHOT
C2 56
R46 10K
R62 1000
R49 1000
R48 1000
PRESET PULSES TO 1μS AND 10μS SWITCHES S1A AND B
Q8 1854-0018 PRESET AMPLIFIER NO. 1
CLOCK COMMON
(1)


PART OF A5 DIGITAL DIVIDER ASSEMBLY (05065-6084)(NOTE 1) SERIES 1904
A5A3 PRESET CLOCK BOARD ASSEMBLY (05061-6013) SERIES 1840
PRESET PULSES FROM PRESET AMPLIFIER NO. 2
0.5μS
S1C 100μS
S1D 1mS
S1E 10mS
Q2 1854-0009
Q3 1854-0009
Q4 1854-0009
Q5 1854-0009
IC5 ÷10 1820-0329
IC6 ÷10 1820-0329
IC7 ÷10 1820-0329
IC1C
IC1D
IC2A
1/4 1820-0094
GATE CONTROL
IC10A 1/2 1820-0080
IC11B 1/2 1820-0080
IC10B 1/2 1820-0080
1.3μS
+4.2V
RESET
Q9 1854-0009
Q11 1854-0009
IC12A 1/2 1820-0086
Q6 1854-0009 INVERTER
IC2C 1/4 1820-0094
IC2D 1/4
IC13 1820-0315 GATE AROUND ONE-SHOT
IC12B 1/2 1820-0086
IC17A 1/2 1820-0080
IC17B 1/2 1820-0080
1μS
150nS
1.1μS
1.8μS
GATE PULSE
PRESET PULSES TO 1μS AND 10μS SWITCHES S1A AND B
PRESET PULSES TO 100μS AND 1mS SWITCHES S1C AND D
PRESET PULSES TO 10mS AND 100mS SWITCHES S1E AND F
Q8 1854-0018 PRESET AMPLIFIER NO. 1
Q10 1854-0018 PRESET AMPLIFIER NO. 2
Q12 1854-0018 PRESET AMPLIFIER NO. 3

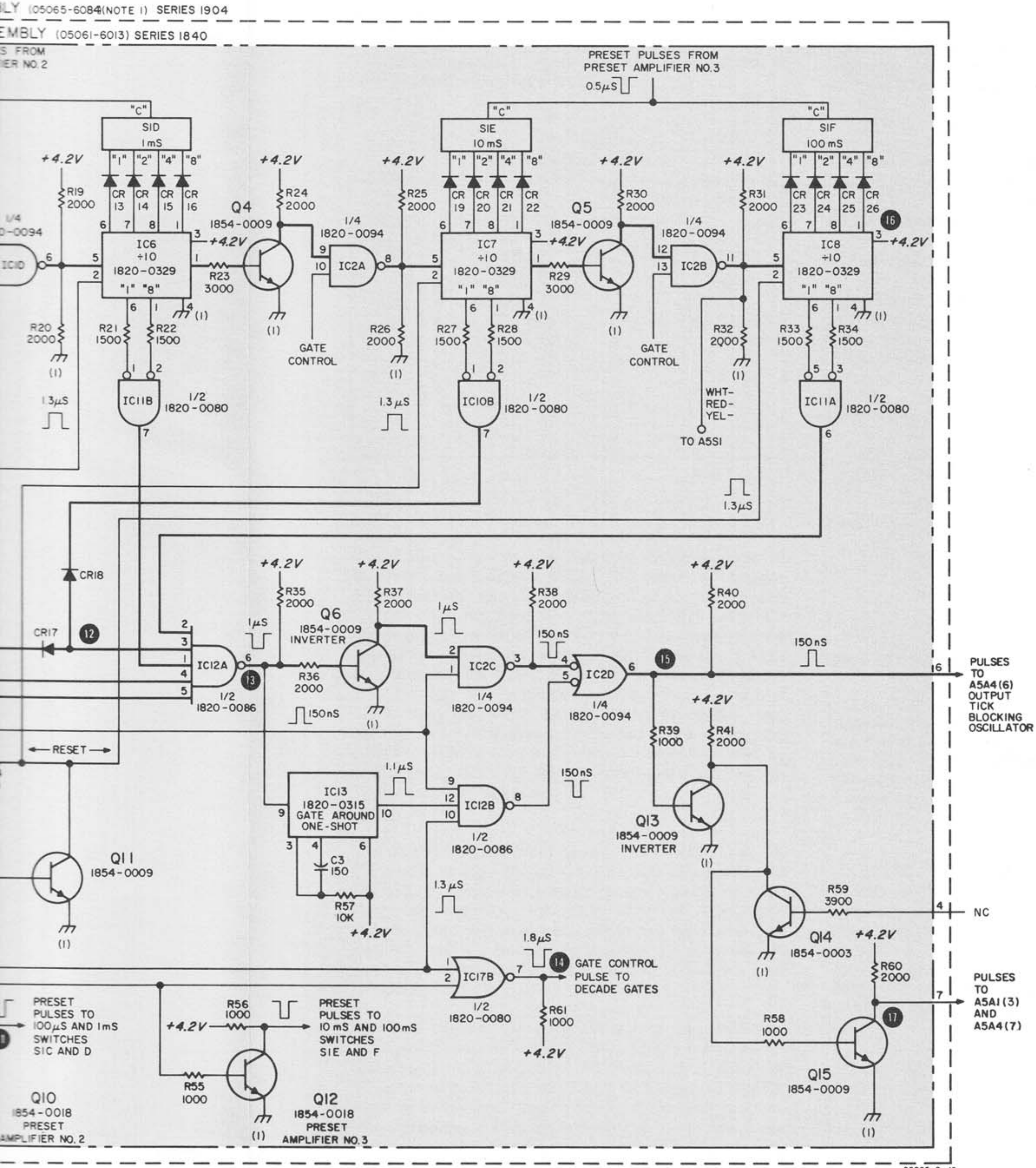
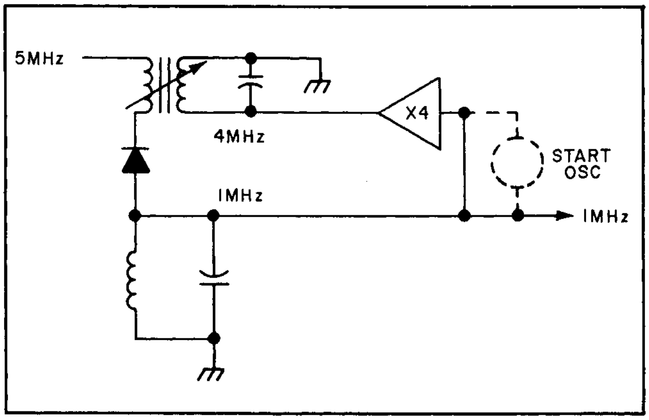


Figure 8-15. A5A3 Preset Clock Board (Option 001)
(Sheet 3 of 3)

1 MHz FREQUENCY DIVIDER A6 THEORY

The A6 module uses regenerative division to divide 5 MHz to 1 MHz as shown in Number 4.

1 MHz Regenerative Divider



The 1 MHz divider is a regenerative divide-by-5 circuit followed by an amplifier stage. This assembly includes signal-sensing logic circuitry to control the divider-start circuits. Assume the 5 MHz signal from A10 Oscillator Assembly is present at the divider circuit input, but the 1 MHz output has not started. Producing the 1 MHz output requires a 1 MHz signal at the base of X4 Multiplier Q4 (this 1 MHz signal is derived from the output signal once the divider starts). Prior to divider start, the required 1 MHz signal is obtained by converting the tuned-amplifier circuit of Q6 into a 1 MHz oscillator by feeding a signal from its output back to its input through field-effect transistor Q5.

The 5 MHz signal input to A6 is amplified by Q1. Capacitive voltage divider C5, C6 couples a portion of Q1 output to the start-circuit detector stage of CR1, CR2, Q2, and Q3. With the START/AUTO-START switch completing a signal path to Q5 base with this switch in either position, the detector stage biases Q5 "on" to complete the feedback path for Q6 which then oscillates at 1 MHz.

Multiplier stage Q4 converts 1 MHz at its base to 4 MHz in its tuned collector circuit. The resulting 4 MHz mixes with the input 5 MHz from T1 in mixing diode CR4. The parallel resonance of L2 and C11 tuned to 1 MHz, traps all undesired frequencies in the mixing product. The remaining 1 MHz couples to Q6 to complete the regenerative feedback path. Sustained regenerative oscillation produces 1 MHz which is amplified by Q8 and Q9. This 1 MHz output is also rectified by CR7 and filtered by C28, R35, and C29 for a dc output to the 1 MHz position of the CIRCUIT CHECK meter.

The 1 MHz output also couples to the start-circuit detector stage of CR5, CR6, and Q7 which sends a dc start signal to start amplifier Q3 for automatic start action with the START/AUTO START switch at AUTO START.

The 1 MHz output to A4 100 kHz Frequency Divider is coupled through C16 from Q6.

A6 MAINTENACE

NORMAL OPERATION

The A6 circuits produce 1 MHz outputs derived by regenerative division of 5 MHz. The A6 Assembly is placed in operation either by placing the START-AUTO START switch in the START position, or by leaving this switch in the AUTO START position whereupon the A6 will start divising 5 MHz when it is applied. A6 outputs are as follows:

a. 1 MHz to front and rear 1 MHz jacks from A6(15).

b. Rectified 1 MHz output to CIRCUIT CHECK meter from A6(12).

c. 1 MHz output to A4(6) from A6(9).

OPERATIONAL CHECK

a. A simple check of A6 operation can be done by observing the CIRCUIT CHECK 1 MHz indication and comparing it with the reference meter readings on the front-panel door. Checking the 100 kHz meter reading will verify that the A6 Assembly is delivering 1 MHz for division to 100 kHz in the A4 100 kHz Frequency Divider.

b. To check operation of the START AUTO-START switch, set this switch at the center-off position and momentarily disconnect A10J4. Note that with the top cover removed, A10J4 is accessible. Without a 5 MHz input to A6, there should be no A6 1 MHz output (or a dc start signal to A4). With A10J4 reconnected, there should be no 1 MHz output until the START AUTO-START switch is placed at either START or AUTO-START.

c. To verify that the 1 MHz output is within specifications, proceed as follows:

1) Using the 5065A 5 MHz output as an external time base input to a counter, connect the 1 MHz front-panel jack to the counter and check for 1 MHz ± 1 count. Disconnect the counter.

2) Connect the front-panel 1 MHz jack through a 50-ohm feedthru to an RF voltmeter. Check for 1.0 to 1.5 volts rms. Disconnect the voltmeter and connect an oscilloscope in its place. Check that the 1 MHz output is a clean undistorted sine wave. Disconnect the oscilloscope.

3) If a distortion check of the 1 MHz output is desired, refer to steps 4 and 5 of Table 5-2, In-Cabinet Performance Check.

TROUBLESHOOTING AND REPAIR

NOTE

For troubleshooting or tuning, the A6 Assembly should be mounted on a HP 05065-6064 board extender. Power should be disconnected before this assembly is removed or reinstalled.

a. Signal Checks

1) To check Q1, Monitor 5 MHz at CR4.

2) To check Q4, disconnect A10J4 to remove 5 MHz and inject 1 MHz (1.0 volts rms) at the junction of R14 and R15. Then check for 4 MHz (1 MHz X4) at CR4. If this checks out, leave the 1 MHz connected, re-establish the 5 MHz connection, and check for a difference 1 MHz CR4 output at the junction of R16 and R18. If everything checks out so far and there is no regenerative division, look for a malfunction in the start circuit of Q5 and Q6. In case the dc start circuit is not working, the start oscillator can be turned on by grounding R8 at pin 6 to close Q5 switch.

b. Tuning Adjustments

1) Connect a 50-ohm termination to the rear panel 1 MHz output jack.

2) Connect a BNC tee to the front panel 1 MHz output jack. Then connect a counter and RMS voltmeter to the BNC tee. Connect the 5065A 5 MHz output to counter EXT STD INPUT and set counter for external standard operation.

3) Set front panel START AUTO-START switch at AUTO START.

4) Tune T1, T2, T3, and C21 for maximum indication on the RMS voltmeter. Counter should indicate 1 MHz ± 1 count.

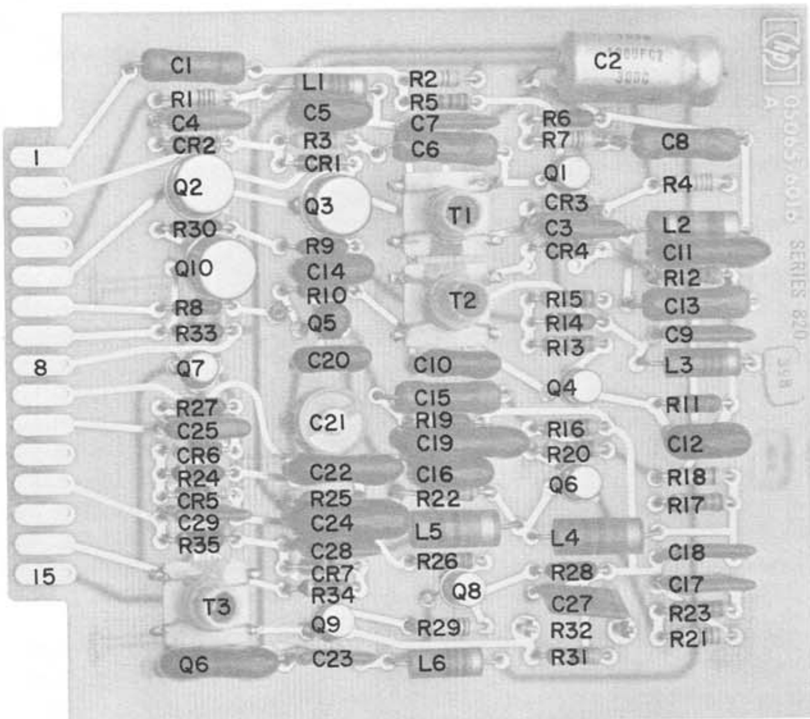
5) Carefully retune A6, T1, T2, T3, and C21 for maximum output. Output level should be between 1.0 and 1.5 volts. This completes the 1 MHz divider tuning.

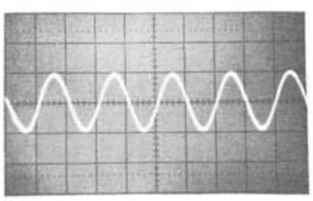
MODULE REPLACEMENT

When replacing the A6 Assembly after repair or when a new A6 Assembly is installed, the instrument should be completely realigned per the preceeding paragraphs.

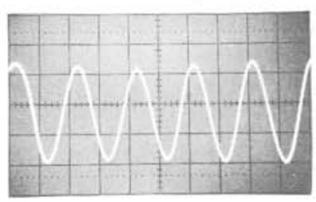
Figure 8-16
A6 1 MHz FREQUENCY DIVIDER ASSEMBLY

(See Page 8-41)

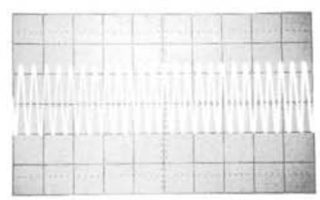




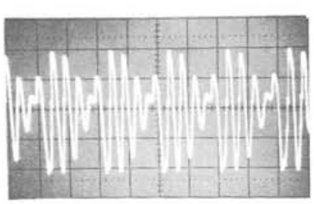
❶ .1 V/cm, .1 μs/cm



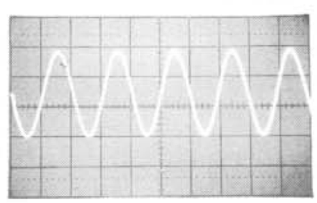
❷ 1 V/cm, .1 μs/cm



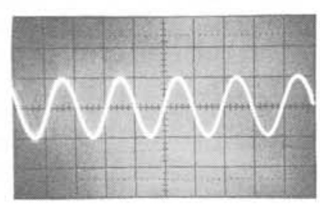
❸ .5 V/cm, .5 μs/cm
(DIVIDER INOPERATIVE)



❹ .5 V/cm, .5 μs/cm
(DIVIDER OPERATIVE)



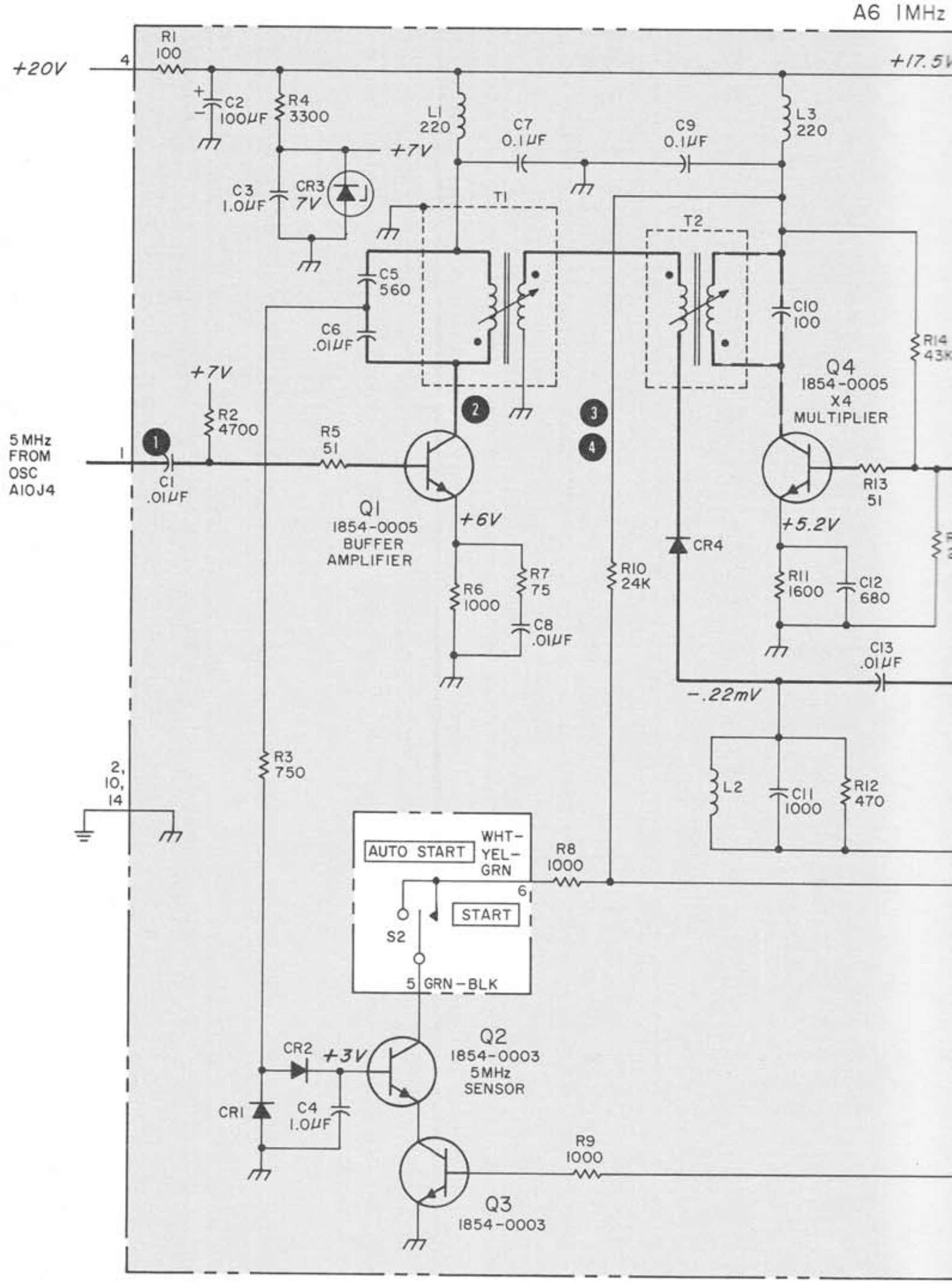
❺ 2 V/cm, .5 μs/cm



❻ 2 V/cm, .5 μs/cm

5065A: Normal operation unless noted.

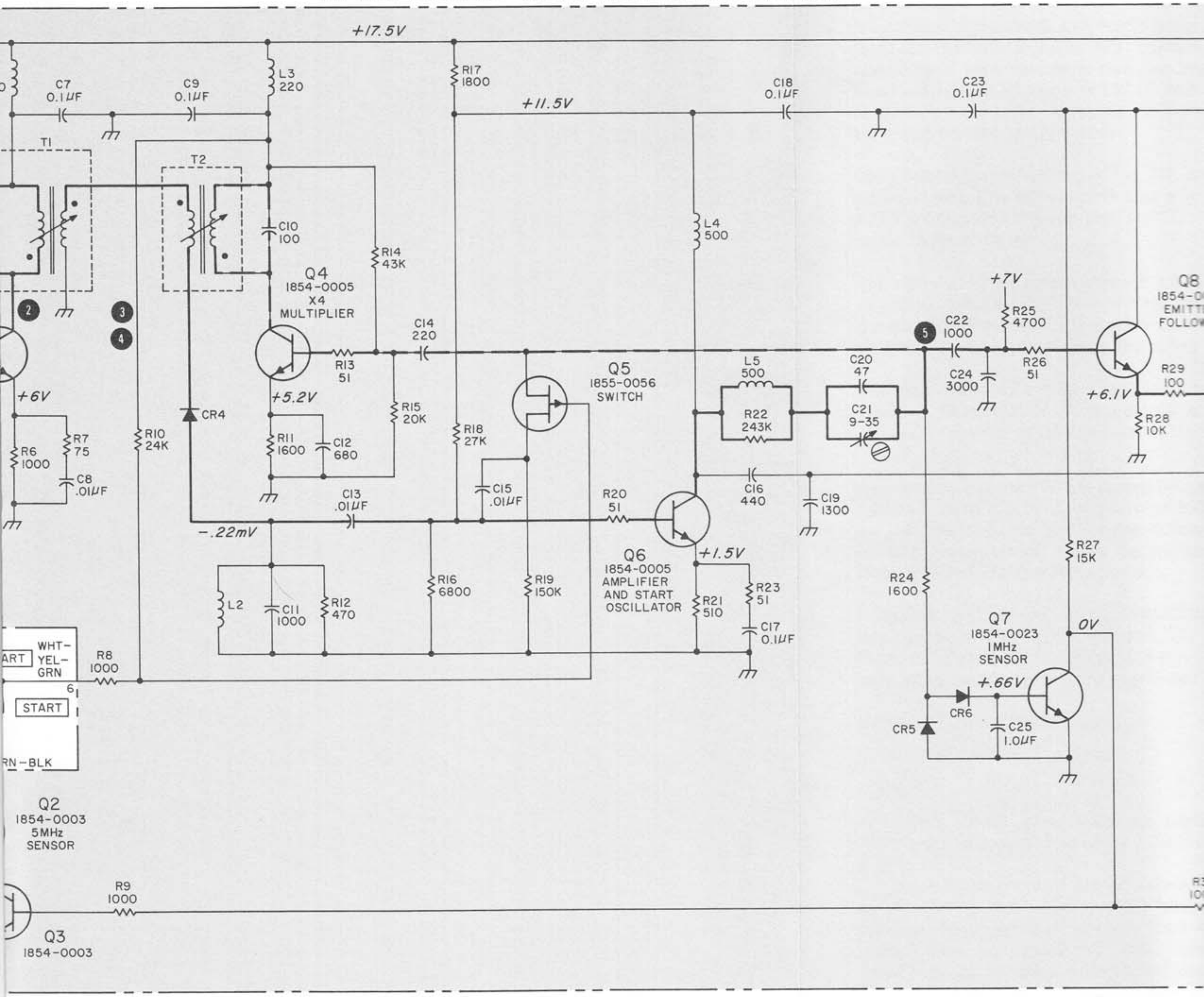
Oscilloscope: DC coupled



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN.

A6 1MHz FREQUENCY DIVIDER ASSEMBLY (05065-6016) (NOTE 1)



NOTES

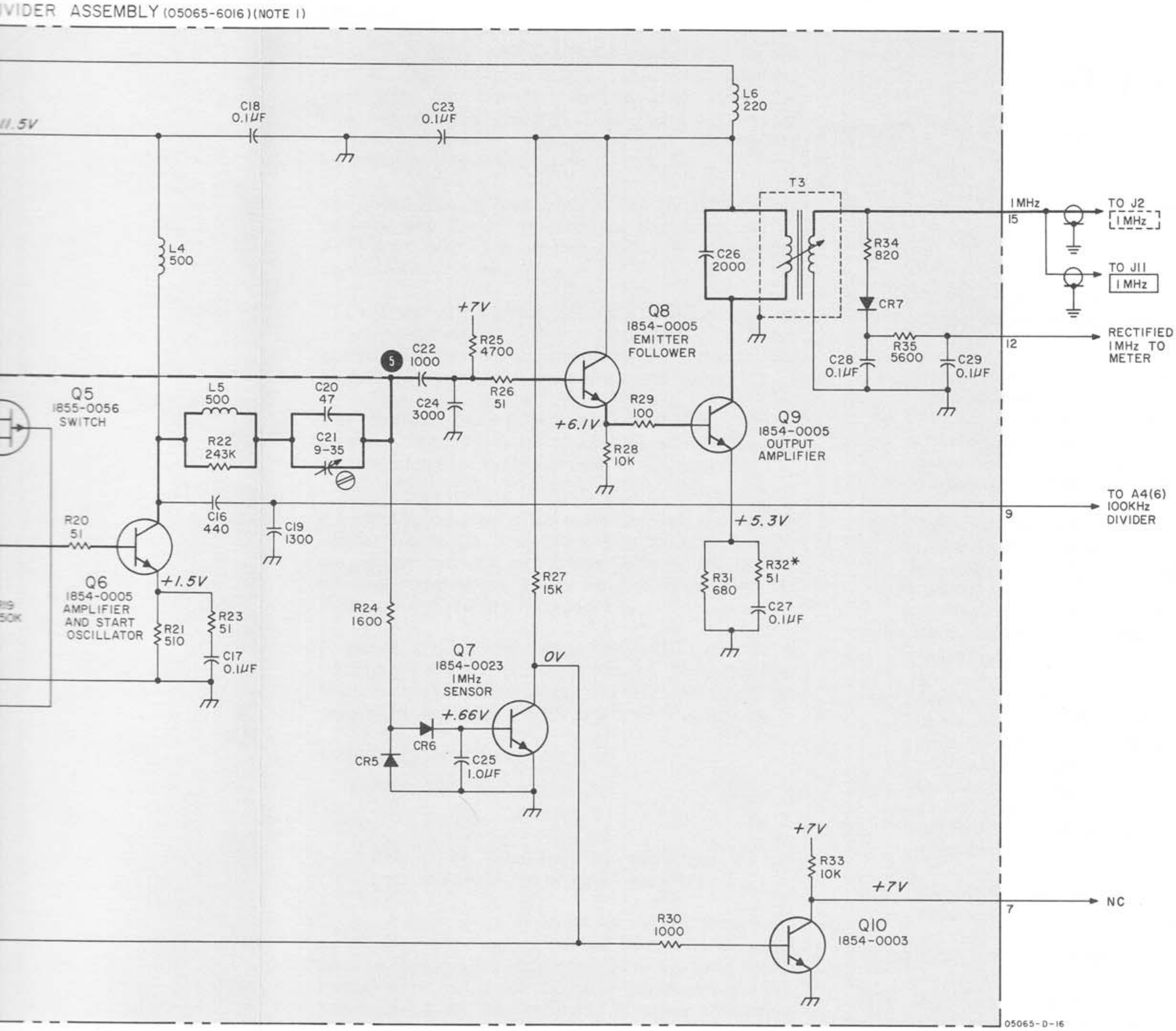
DESIGNATIONS WITHIN THIS
ARE ABBREVIATED. ADD
NUMBER TO ABBREVIATION
ETE DESCRIPTION.

HERWISE INDICATED:
CE IN OHMS;
NCE IN PICOFARADS;
CE IN MICROHENRIES

) INDICATES SELECTED
, AVERAGE VALUES SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A6
S2	C1-29 CR1-7 L1-6 Q1-10 R1-35 T1-3



REFERENCE DESIGNATIONS

NO PREFIX	A6
S2	C1 - 29 CR1 - 7 L1 - 6 Q1 - 10 R1 - 35 T1 - 3

Figure 8-16. A6 1 MHz Frequency Divider Assembly

AC AMPLIFIER A7 THEORY

THEORY

A low-level signal from A12 RVFR assembly is applied to A7J1. The input signal to A7J1 contains the ac and dc components from the photo-detector inside the RVFR. The fundamental ac signal is 137 Hz and is proportional to the frequency error. A second-harmonic signal to 274 Hz is also present at A7J1 input.

The preamplifier consisting of Q1, Q2, and IC1 is a low noise dc amplifier with a zero bias adjustment (A7R3) A7R3 is adjusted for 0 Vdc bias at A7Q1(B) to minimize noise on the A7J1 input.

The signal at IC1(6) is sent through a 274 Hz notch-filter to emitter-follower Q5. The 274 Hz notch-filter, filters out the second harmonic component, and allows the 137 Hz fundamental signal to pass through to Q5 and IC2.

The amplified output from IC2(6) is routed to A8 Phase Detector. A portion of the IC2 output is sent through a 137 Hz notch-filter to Q6 and used as feedback to IC2.

A second output from IC1(6) is sent through level adjustment A7R29 to IC3. The output from IC3 goes through the rectifier network and emitter-follower Q9 to A17 terminal board where it may be monitored when M1 meter is in 2ND HARMONIC position.

Feedback around the 2ND HARMONIC amplifier is through the 274 Hz Notch-filter and Q7. Since the filter feeds back all frequencies but 274 Hz. The amplifier's gain is high at 274 Hz and low at all other frequencies.

OPERATIONAL CHECK

NOTE

This check need only be performed if trouble is suspected in the A7 Assembly.

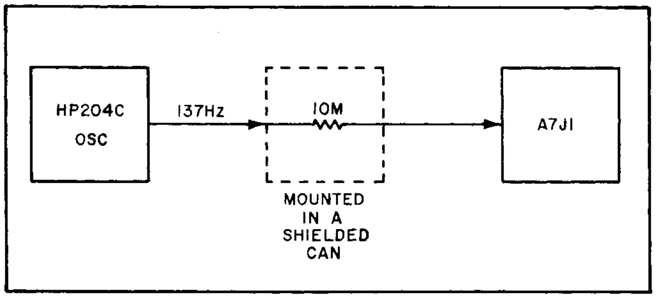
a. A quick check of the A7 Assembly can be made by monitoring the output (yellow lead) with an oscilloscope. Remove the input cable from A7J1 and, using a small metal tool, touch the center conductor of A7J1. The "hum signal" thus induced will cause a saturated signal to appear on the oscilloscope. This maximum signal output will peg the CIRCUIT CHECK meter when switched to 2ND HARMONIC.

b. A more precise test can be made using the following procedure.

1) Set up equipment as shown in A7 Test Setup. Use Micon-to-BNC test cable that is supplied, for the connection to A7J1.

2) Set oscillator frequency to 137 Hz and output level to .5 V peak-to-peak.

A7 Test Setup



3) Connect oscilloscope to A7TP2 or A7WBB. Output should be about .9 V peak-to-peak.

4) Connect oscilloscope to A7 output (Yellow lead). Signal gain can be varied from zero to the point where the amplifier clips at about 16 V peak-to-peak by varying R17. With R17 set for proper loop gain, the A7 output signal will be roughly 6-7 times the signal at A7TP2.

5) Set CIRCUIT CHECK meter switch to 2ND HARMONIC. Reduce oscillator output and allowing for a time lag, note the CIRCUIT CHECK meter response. Meter should follow oscillator level setting. This procedure checks the second harmonic detector circuit of the A7 Assembly.

6) Remove the test setup and oscilloscope connections. Using the Micon-to-BNC test cable provided, connect a dc voltmeter to A7J1. Dc voltage at this point should not exceed ± 5 mV. Excessive dc voltage at this point will result in a noisy solar cell (A12 RVFR Assembly) output. Adjust A7R3 to bring this voltage below ±5 mV if required.

7) Remove test cable and dc voltmeter. Reconnect cable from A12 Assembly to A7J1.

TROUBLESHOOTING AND REPAIR

a. If any components in the preamplifier circuit are replaced, connect a voltmeter to A7Q1 base and adjust A7R3 for less than 0.5 mV at this point.

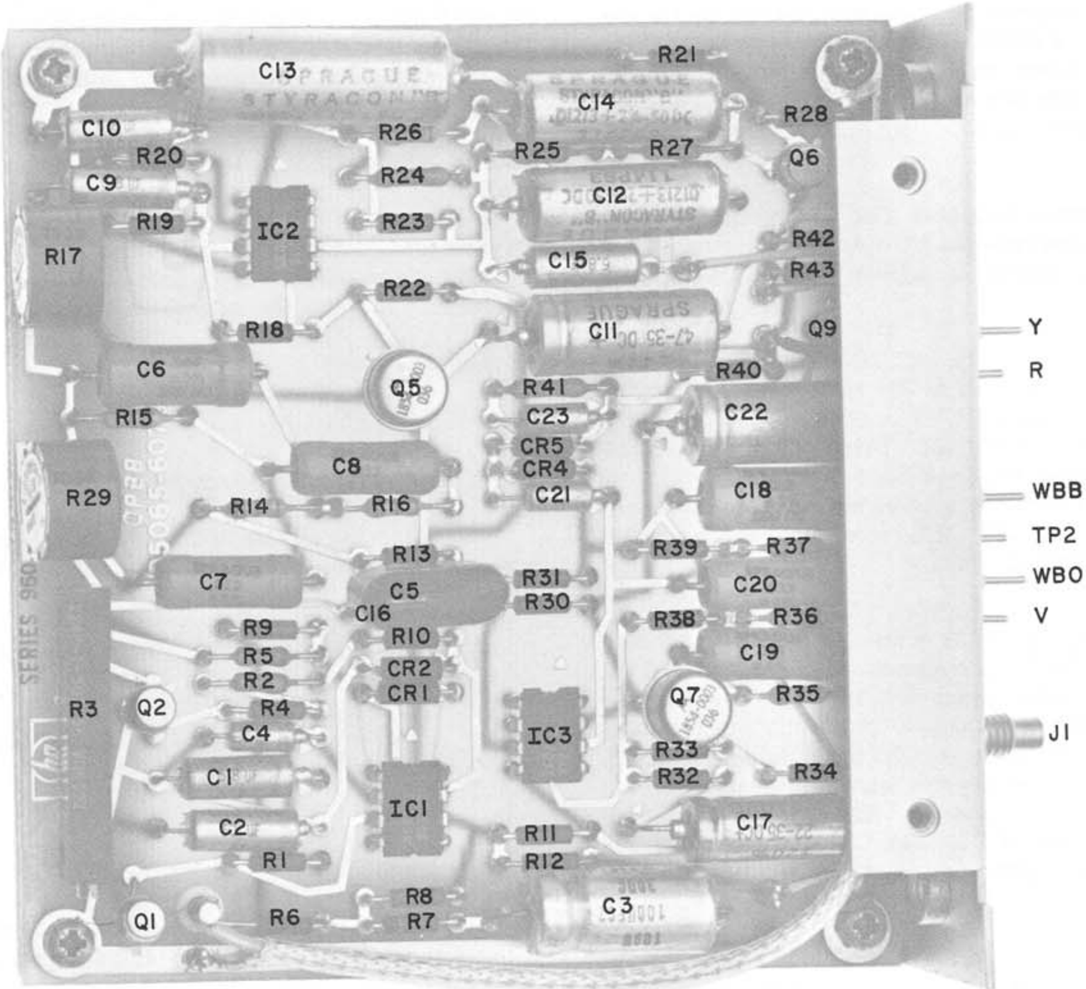
b. After any repairs to A7 Assembly, adjust A7R17 as described in Section 5-30, LOOP GAIN ADJUSTMENT.

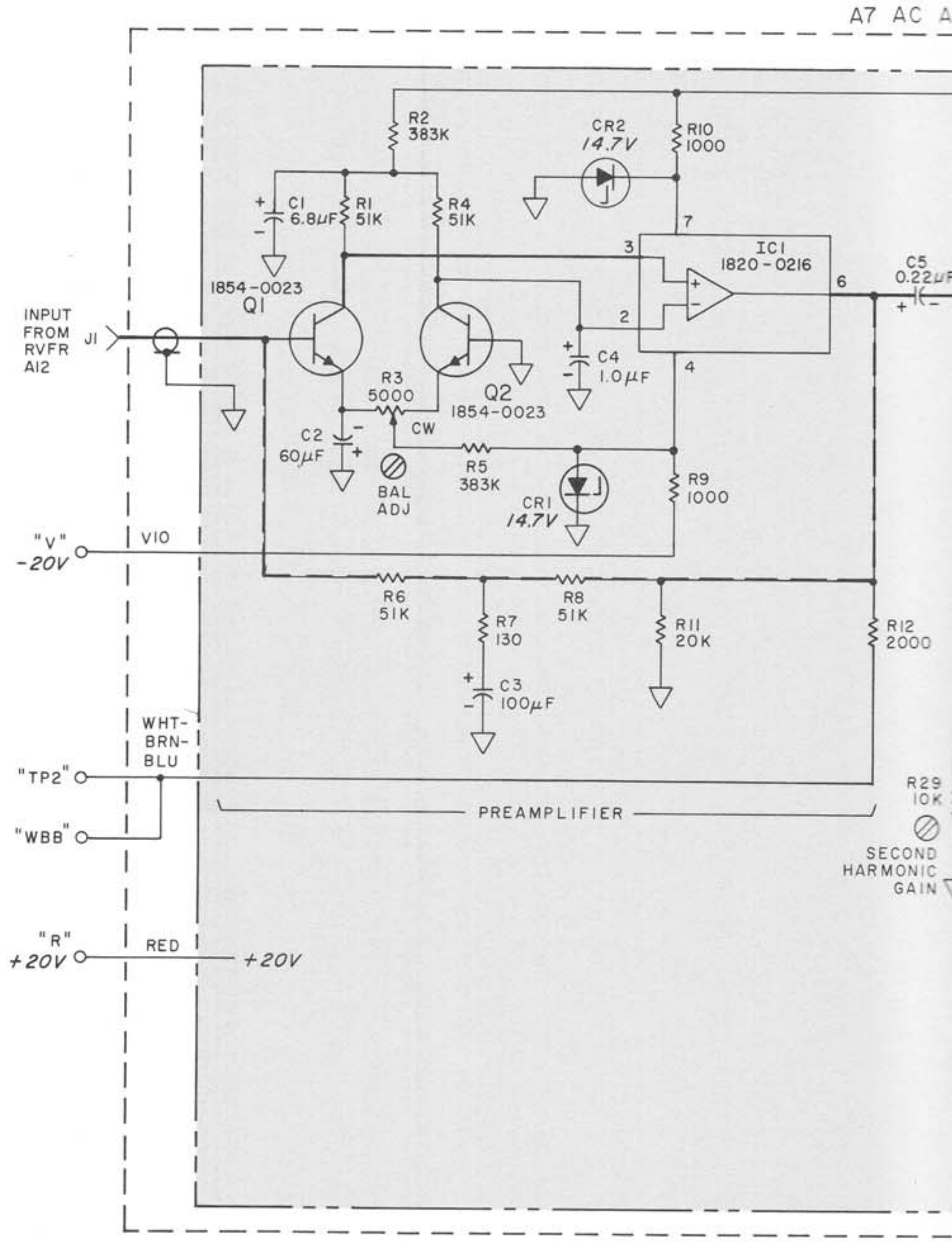
MODULE REPLACEMENT

If the A7 Assembly is replaced with either a repaired or new Assembly, set A7R3 as described in the preceding section TROUBLESHOOTING AND REPAIR. Also perform adjustments outlined in Paragraphs 5-27 to 5-31.

Figure 8-17
A7 AC AMPLIFIER ASSEMBLY

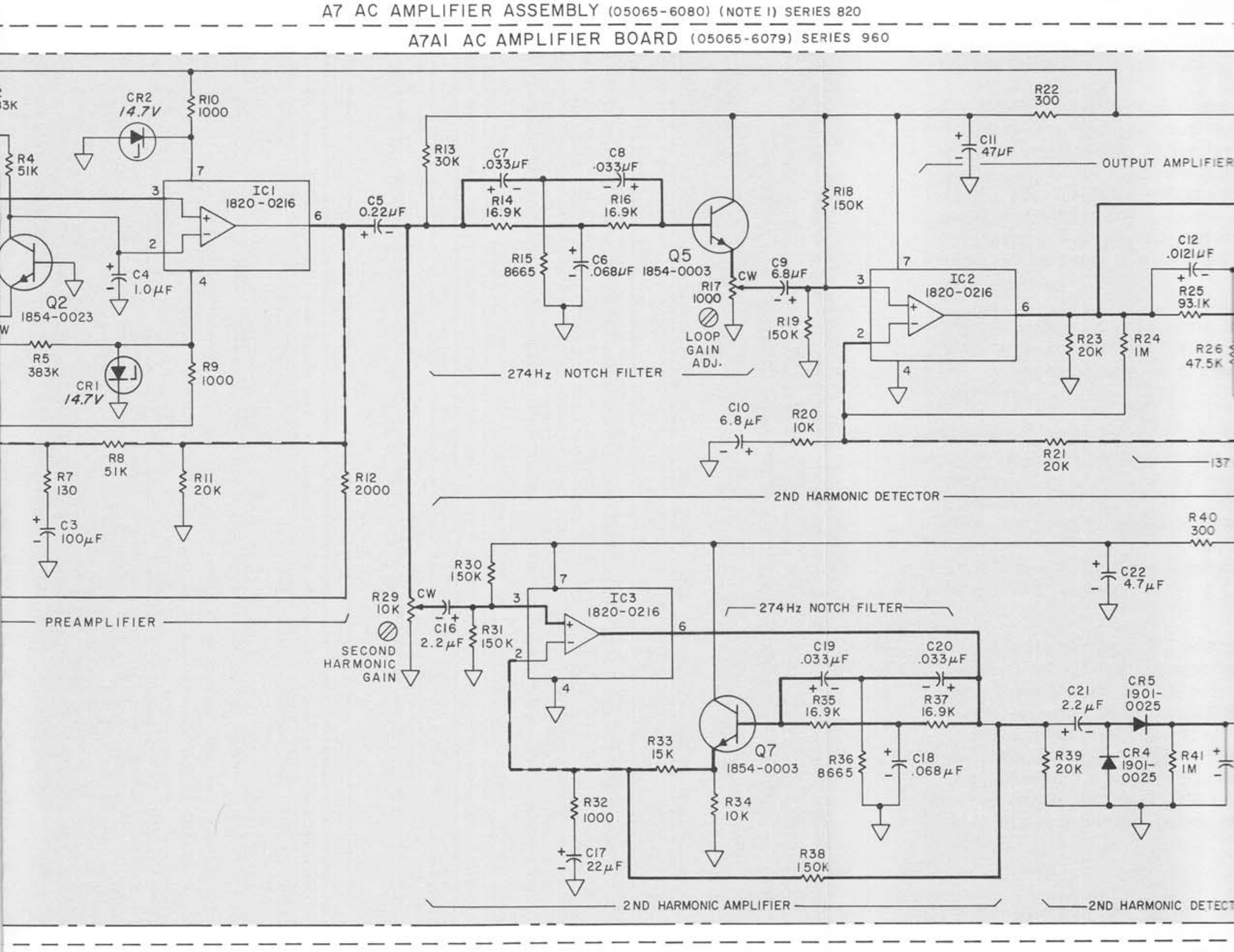
(See Page 8-43)


C13
R21
C14
R28
C10
R26
R25
R27
Q6
R20
R24
C9
C12
R19
IC2
R23
R42
R17
C15
R43
R22
R18
C11
Q9
Y
R40
R
C6
Q5
R41
C22
R15
C23
CR5
C8
CR4
R29
C18
WBB
R14
R16
C21
R39
R37
TP2
R13
C7
C5
R31
C20
WBO
R30
C16
R38
R36
V
R9
R10
C19
R5
CR2
R2
CR1
Q7
R35
R3
Q2
R4
C4
IC3
J1
R33
C1
R32
R34
IC1
C2
C17
R11
R1
R12
R8
C3
Q1
R6
R7
SERIES 960



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

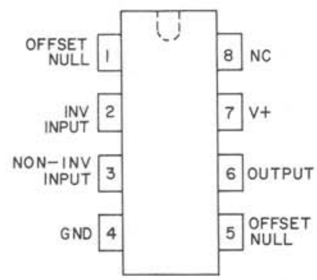


NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

A7	A7A1
J1	C1-23 CR1,2,4,5 IC1-3 Q1,2,5-7,9 R1-43



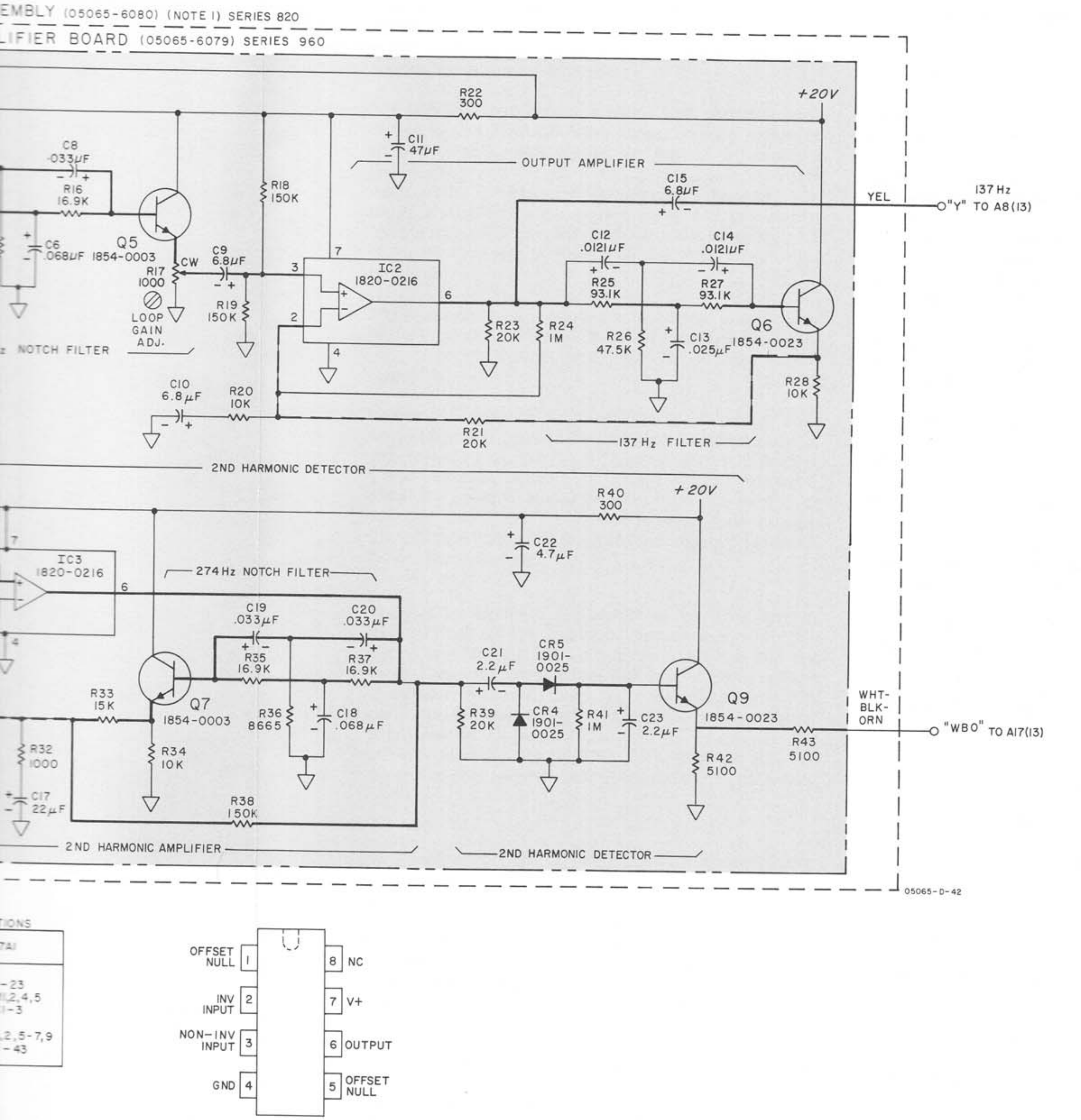


Figure 8-17. A7 AC Amplifier Assembly

PHASE DETECTOR ASSEMBLY A8 THEORY

Separate functions in A8 Phase Detector Assembly are shown in the A8 block diagram. The two basic circuits in this assembly are the modulation reference oscillator and the 137 Hz phase detector.

The reference oscillator is a phase shift oscillator producing a 274 Hz sine wave output. This signal is shaped in a Schmitt trigger for driving a frequency divider. The frequency divider output is a 137 Hz square wave applied to a phase shifter and phase detector. The phase shifter filters the square wave and provides a 137 Hz signal with very low 2nd Harmonic content to A3 Multiplier Assembly to modulate the 5 MHz quartz oscillator signal.

The phase detector produces a dc voltage proportional to the error signal received from Ac Amplifier Assembly A7. This dc output is applied to A9 Operational Amplifier.

Reference oscillator Q1, Q2, Q3 is a phase shift oscillator which operates at 274 Hz. The frequency is determined by C1, C3, R4, R7, and R8 with R8 providing a fine frequency adjustment. These components complete the positive feedback loop from Q3 to Q1 to maintain oscillation. A second feedback loop through CR1, CR2, R5, R6, and C2 provides negative feedback for amplitude limiting.

The 274 Hz signal at Q3 emitter is fed to a Schmitt trigger circuit Q4, Q5, and associated components. This circuit is a shaping circuit with very fast rise and fall times. Capacitor C7 bypasses R14 to couple fast voltage changes from Q4 collector to Q5 base. Either Q4 or Q5 conducts, the negative-going transition at its collector is supplied to the frequency divider (÷ 2) circuit. The network composed of C8, CR3, C11, R18, and R20 ensures that only negative pulses are fed to the frequency divider.

Frequency divider Q6, Q7 is a binary divider producing an output pulse after receiving two input pulses from Q5. A negative pulse from Q5 is applied to Q6 or Q7 base through gating diodes CR4 or CR5. This negative pulse turns off the conducting transistor. Capacitor C13 provides filtering for Q6, Q7 emitters and R25 establishes a small voltage at the common emitter junction to ensure that one of the two transistors is cut off.

The phase shift network includes Q8, Q9, and associated components, and allows phase adjustment of the 137 Hz sine wave. This phase shift is necessary to establish the correct relationship between the modulating 137 Hz and the 137 Hz reference sent to the phase detector. Phase adjustment control R43 provides the phase adjustment. Because the signals driving transistors Q8 and Q9 are symmetrical square waves, second harmonic content is very low (zero for perfect symmetry). Components R45, C24, R47, and C25 provide low pass filtering. The signal output is a 137 Hz sine wave with second harmonic distortion at least 80 dB below the signal level.

Phase detector Q12A, B, and associated components receive two inputs: (1) the 137 Hz reference square wave through Q10 and Q11 and, (2) the error signal from Ac Amplifier Assembly A7. The output is a dc error signal supplied to Operational Amplifier A9. Emitter followers Q10 and Q11 drive the phase detector. Transistors Q12A, B are alternately turned on and off by the 137 Hz reference square wave. The ac error signal is applied to T1 secondary. The phase detector output at T1 primary center tap is the dc error signal which goes to A9 Operational Amplifier. Potentiometer R35 is a dc zero adjustment.

Q11 output is integrated to a triangular wave by R42 and C21 for an oscilloscope signal at TP2. This signal can be used to check Q11 square wave output.

A8 MAINTENANCE

NORMAL OPERATION

Phase detector circuits provide the following outputs:

a. 130 to 142 Hz, 80 to 250 mV peak-to-peak sine wave to A3J1. This is phase modulation to A3 Multiplier Assembly.

b. 130 to 142 Hz, 1.5 to 2.1 V peak-to-peak triangular wave at A8TP2.

c. Dc error signal outputs at A8(11), A8(14), and A8TP3 which are used by A17 and A9.

NOTE

When 5065A is operating normally (Atomic loop closed) the error signal at A8(14) is very small (mostly noise).

OPERATIONAL CHECK

To determine if Phase Detector Assembly is operating normally perform the following checks:

a. Operation mode of 5065A is not important for this check. Connect an oscilloscope vertical input to A8(9). Waveform should be as in 8.

b. Set FUNCTION switch to OPER. Connect a frequency counter to A8TP2. Frequency should be between 130 to 142 Hz. Do not adjust frequency if these limits are met. If frequency is outside 130 to 142 Hz adjust A8R8 for 137 Hz.

c. Set unit controls:

1) FUNCTION to LOOP OPEN OSC FREQ ADJ FINE to 250. Connect oscilloscope vertical input to A8TP3. Connect oscilloscope horizontal input to sweep test output A8TP2. Set horizontal gain for a 5 cm sweep. Set vertical gain to .5 V/cm.

2) Adjust OSC FREQ ADJ COARSE until oscilloscope pattern is similar to the unadjusted A8TP2 Output. Display is indication that unit is tuned near resonance.

d. When unit is tuned through resonance, oscilloscope pattern changes from positive hump to a line (at resonance center) then to a negative hump. Unit should be adjusted for straight-line resonance indication between humps.

e. Set OSC FREQ ADJ FINE to 200 (50 x 10^{10} frequency offset). Oscilloscope pattern should be similar to the Optimized A8TP3 Output.

f. Remove yellow wire from A7 Assembly. Check phase detector zero with voltmeter at A8TP3. Reading should be 0 V ± 1 mV. If not, adjust A8R35.

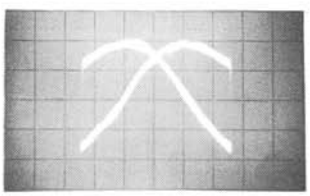
TROUBLESHOOTING AND REPAIR

When any components are repaired or replaced the assembly should be adjusted. If Rubidium vapor assembly is replaced, phase detector circuits should be readjusted. For complete adjustment perform paragraphs 5-25, 5-27 through 5-30.

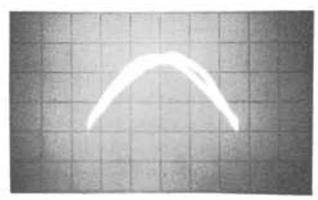
MODULE REPLACEMENT

Phase detector module may be replaced with power on. After replacement new module should be adjusted per paragraph 5-29.

Unadjusted A8TP3 Output



Optimized A8TP3 Output



Phase Detector Block Diagram

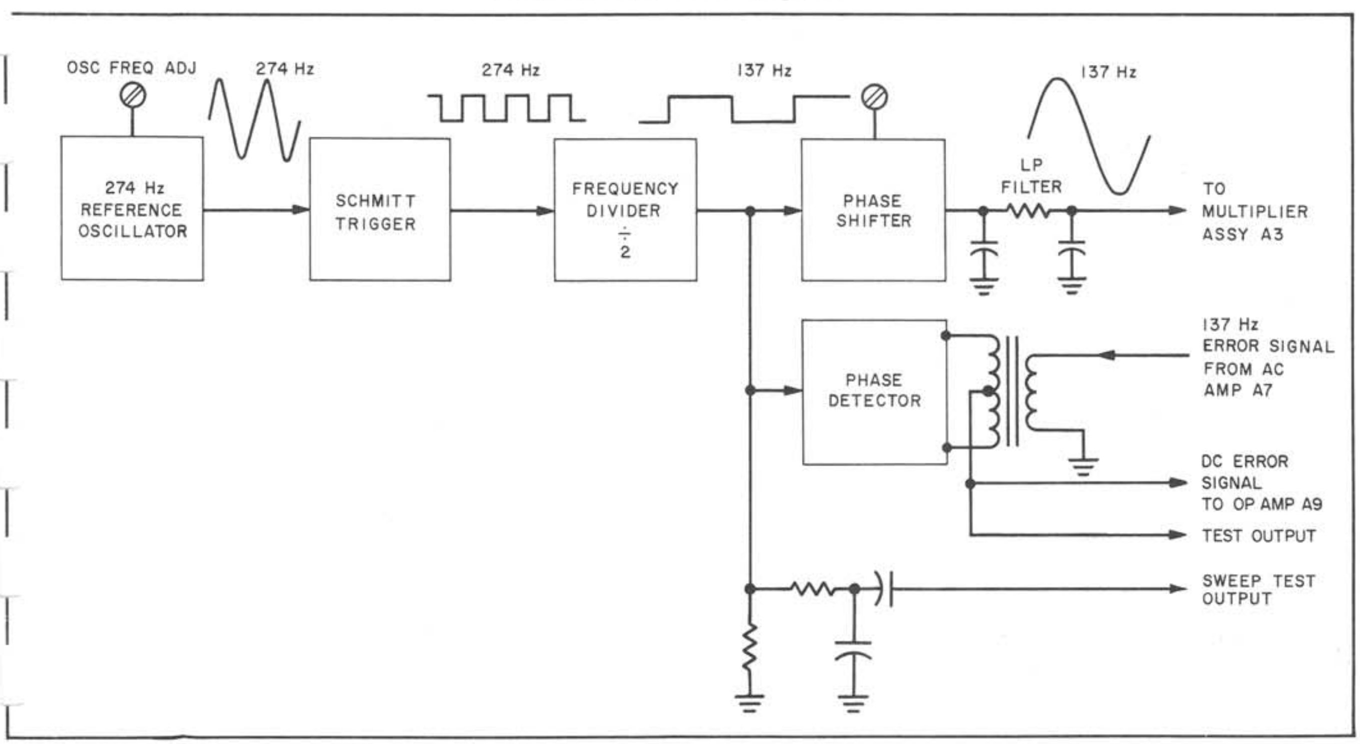
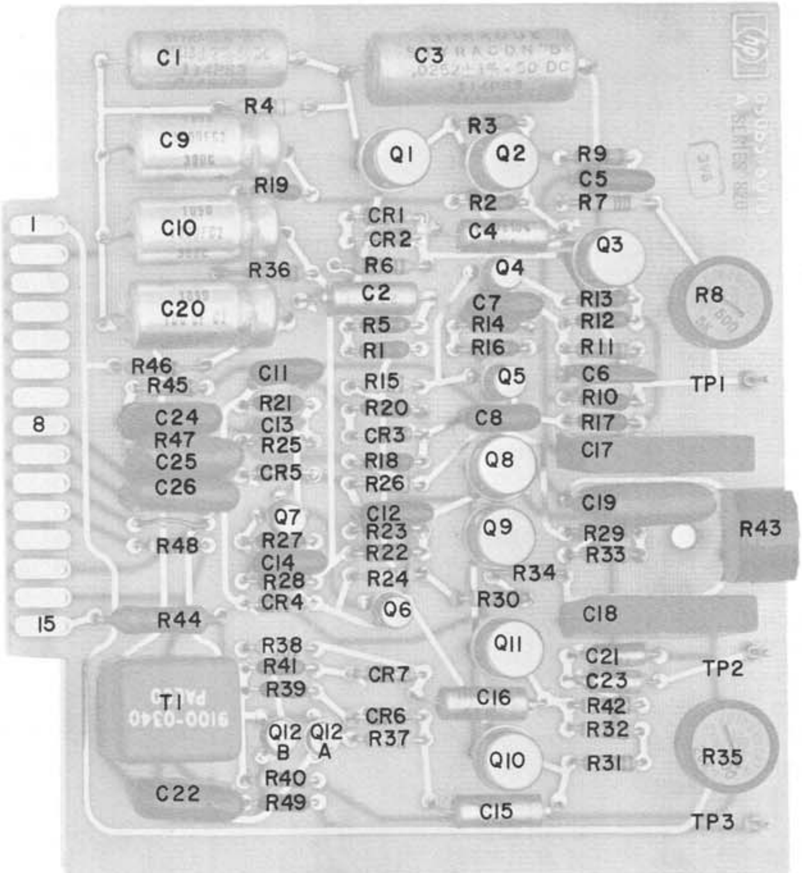
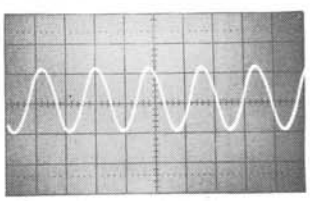


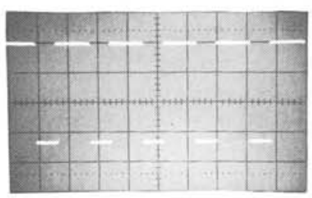
Figure 8-18
A8 PHASE DETECTOR ASSEMBLY

(See Page 8-47)

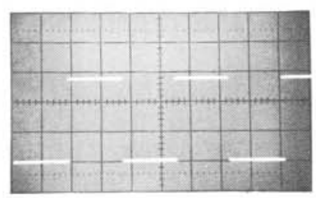




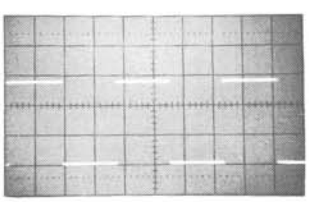
1 2 V/cm, 2 ms/cm



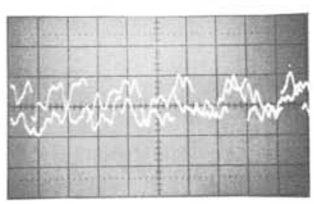
2 5 V/cm, 2 ms/cm



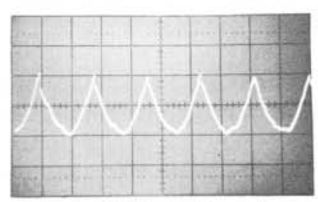
3 5 V/cm, 2 µs/cm



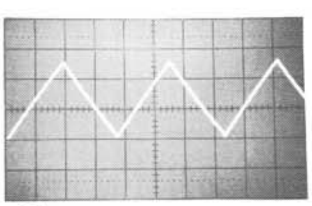
4 5 V/cm, 2 µs/cm



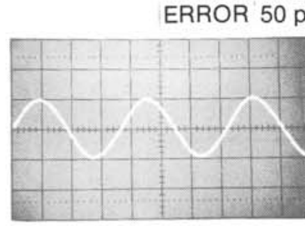
5 .1 V/cm, 2 ms/cm (System Locked)



6 .5 V/cm, 2 ms/cm (LOOP OPEN, FREQ ERROR 50 parts in 10^{10})



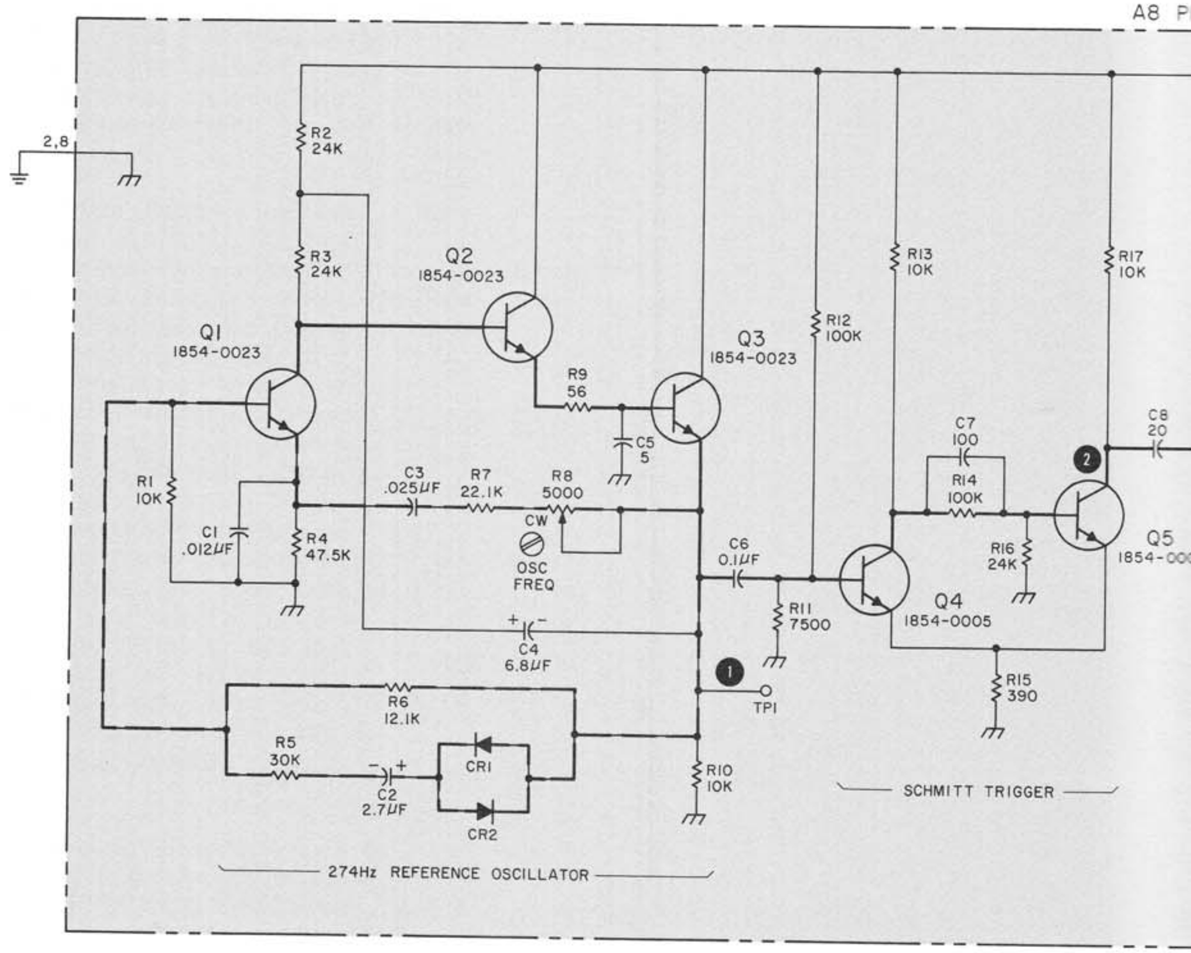
7 .5 V/cm, 2 ms/cm



8 .1 V/cm, 2 ms/cm

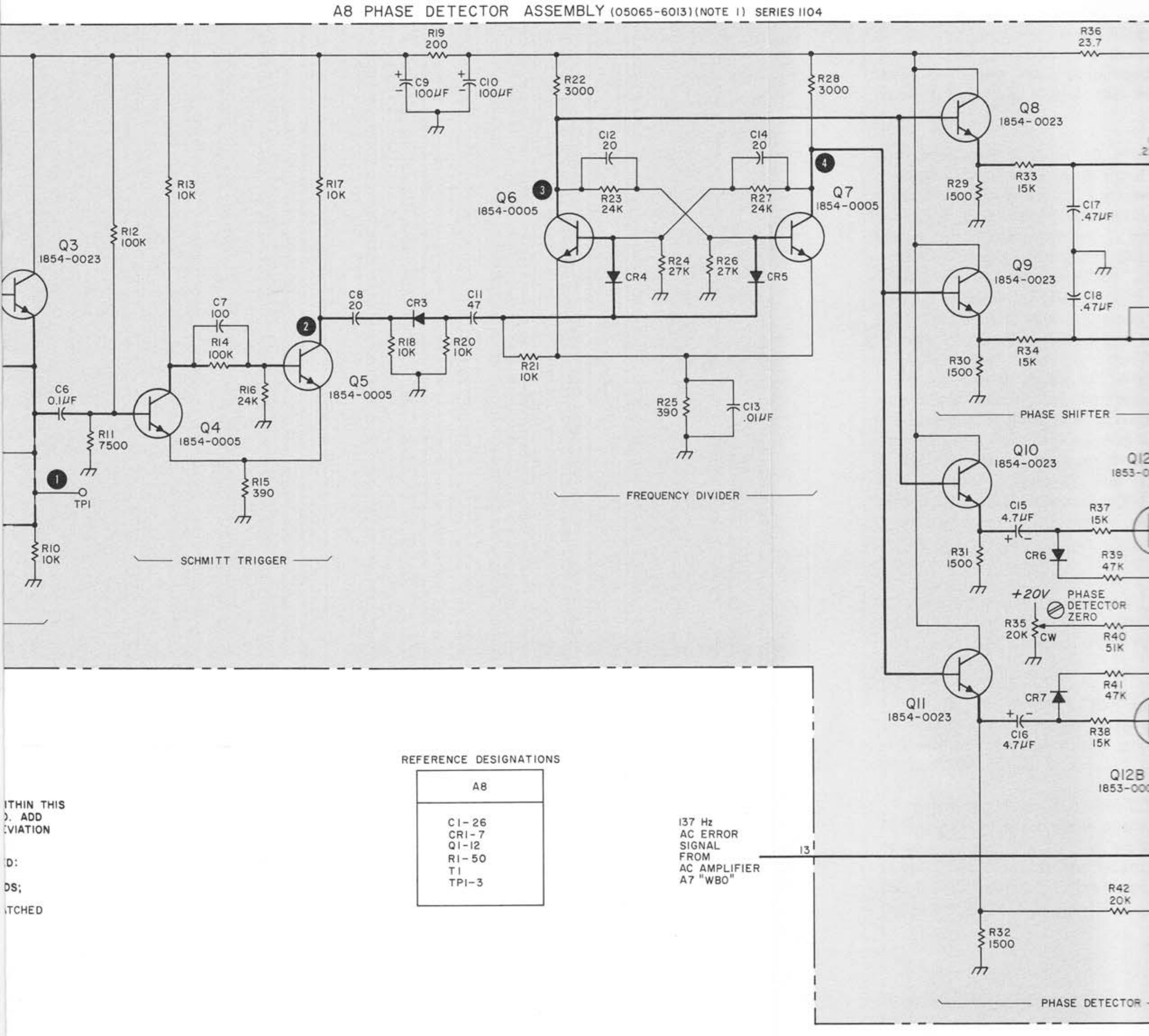
5065A: Normal operation unless noted.

Oscilloscope: DC coupled



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
3. Q12A AND Q12B ARE A MATCHED PAIR.



REFERENCE DESIGNATIONS

A8
C1-26 CR1-7 Q1-12 R1-50 T1 TP1-3

ITHIN THIS
). ADD
VIATION

D:

DS;

TCHED

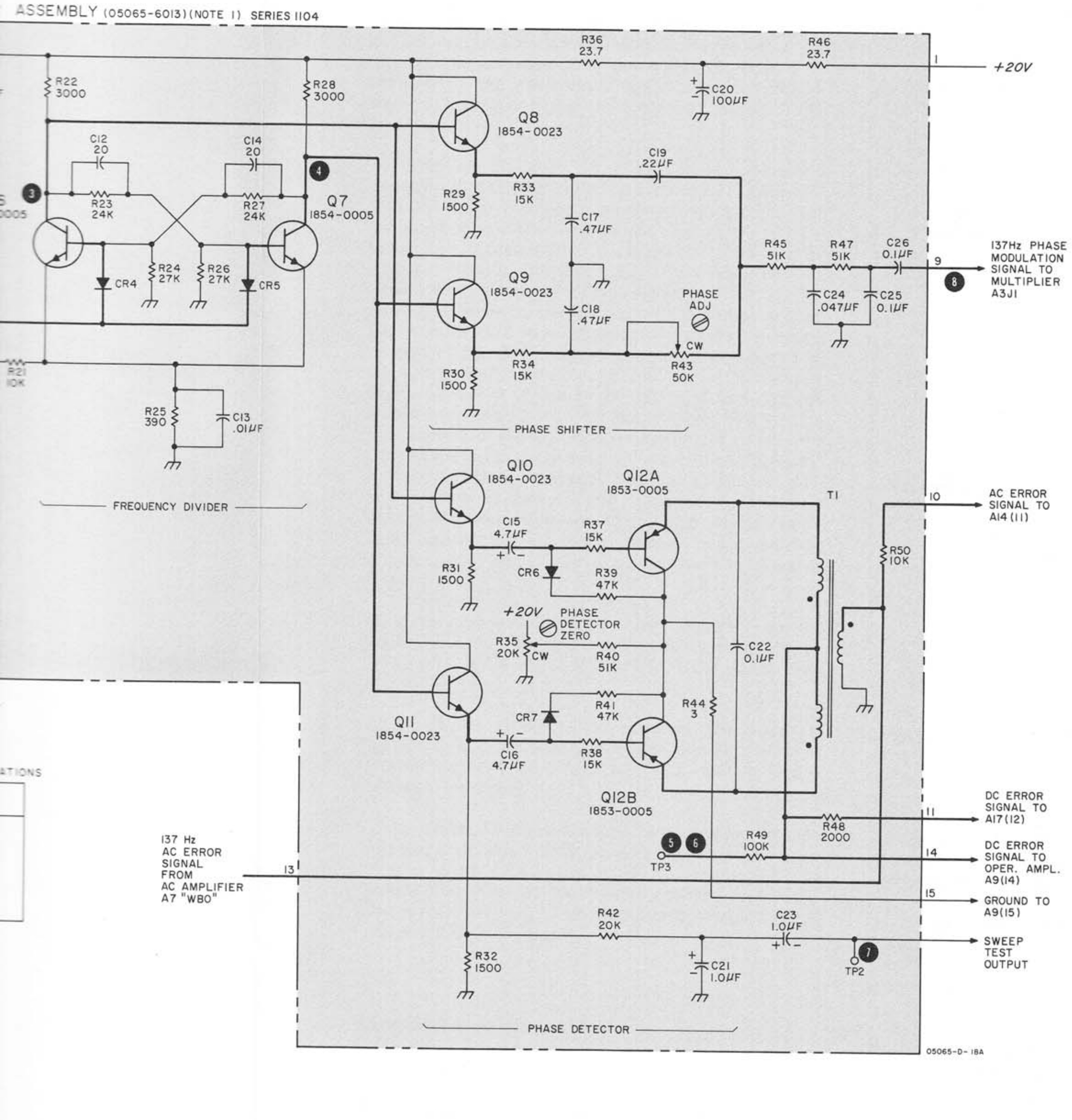


Figure 8-18. A8 Phase Detector Assembly

OPERATIONAL AMPLIFIER A9 THEORY

The A9 Assembly amplifies and integrates the output of A8 Phase Detector and provides a dc error signal for controlling the quartz oscillator in A10 Assembly. The FUNCTION switch provides a means of opening the control loop by shorting the A9 output to its input and placing a large resistance in series with the output. In addition to the integrating feedback, an amplitude-limiting feedback signal prevents saturation of A9 amplifier circuits.

Dc error signals from A8 Phase Detector connect through pin 14 to Q1A, B input amplifier. This FET amplifier stage provides a high-impedance input and push-pull outputs to differential amplifier AMPL1. Balancing adjustments are: Integrator Zero Coarse Adjustor R3 and Integrator Zero Fine Adjustor R10. Zener diode CR1 provides regulated 10 volts for AMPL1. Further dc amplification is handled by Q2 and Q3. Diodes CR6 and 7 provide the proper operating voltage for Q3. The integrating function is provided by C3 (Q3 output connects through C3 to Q1A input). Output signals in excess of ±14 volts feed back through reverse connected clamping Zener diodes CR8 and CR9. That portion of the signal in excess of ±14 volts is fed back to the input at Q1 base to limit signal amplitudes in the A9 circuits, thus providing the A9 circuits with fast overload recovery. The feedback signal routes through the diode network of CR2, 3, 4, 5. These diodes, series connected for each polarity, give isolation between input and output when no overload signal is present.

Q3 output connects to the A14 Logic Assembly as one logic input and to the CONTROL position of the CIRCUIT CHECK switch. The FUNCTION switch does two things:

a. In the OPEN LOOP position, Q3 output is shorted to Q1A input for unity gain and R5 (100K) is inserted between Q3 output and A10 input to further attenuate the signal.

b. In the OPER position, Q3 output feeds through R23 and CR10 which limits positive signals to the range of zero to +7 volts. This signal routes through the FUNCTION switch to the quartz oscillator control circuit in A10 Assembly. This output also connects to the rear-panel CONTROL jack.

A9 MAINTENANCE

NORMAL OPERATION

The integrating amplifier uses the error signal from the phase detector as an input and provides the control voltage for the Quartz Oscillator Assembly A10. The output voltage swing is clamped between -14 Vdc and +7 Vdc.

OPERATIONAL CHECK

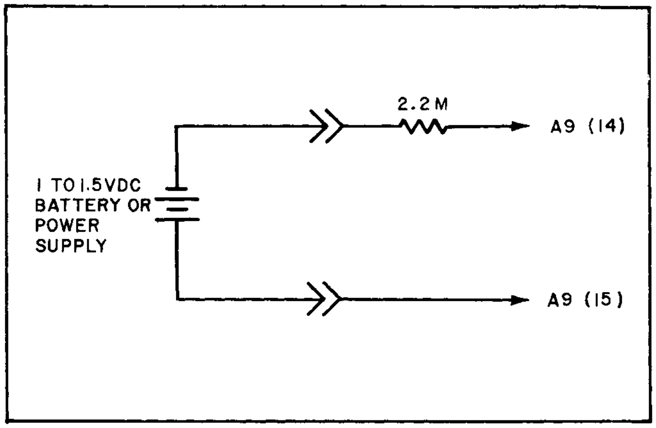
a. Remove A8 circuit board from its socket.

b. Short pins 14 and 15 of A9 Assembly and connect a dc voltmeter to rear panel CONTROL jack.

c. Set FUNCTION switch to LOOP OPEN and then to OPER. Measure voltage on dc meter. This voltage may be drifting, caused by the Integrating Amplifier integrating its internal zero offset. If voltage drift exceeds 20 mV/minute, A9R3 and R10 should be adjusted for minimum drift.

d. Remove short from pins 14 and 15. Set FUNCTION switch to LOOP OPEN and connect circuit as shown:

A9 Test Setup



e. Set dc voltmeter to 30 V range. Observing dc voltmeter set FUNCTION switch to OPER. The voltage will increase at the rate of about 1 V/second to about -14 V.

f. Set FUNCTION switch to LOOP OPEN. The voltage will go to ZERO. Now reverse the battery or power supply connections so that the negative terminal is connected to the 2.2 megohm resistor.

g. Set voltmeter to read positive voltages. Set FUNCTION switch to OPER and observe voltmeter reading. Reading should increase at a rate of about 1 V per second to a final reading of approximately +7 V.

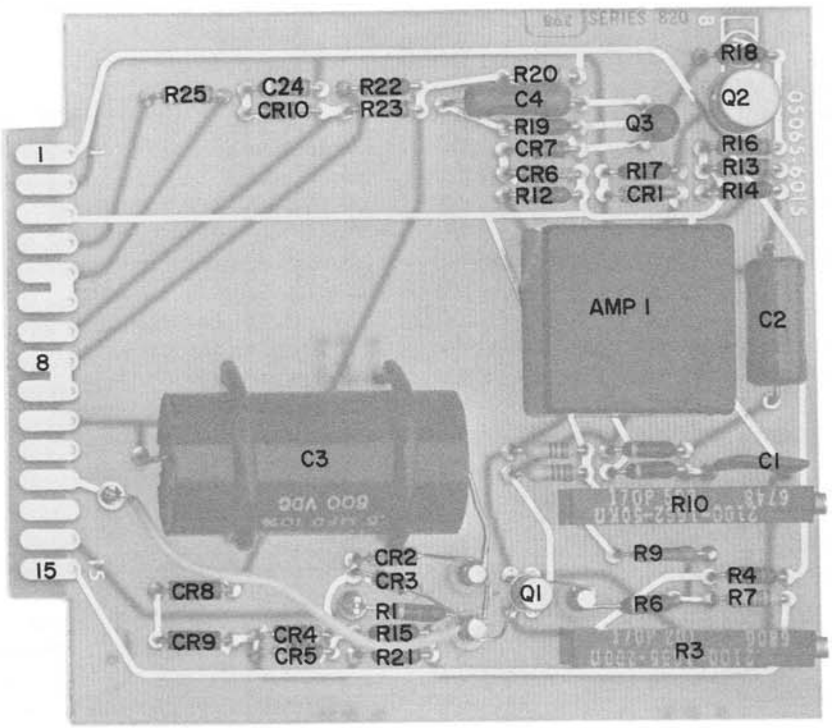
h. Remove connection to A9, pins 14 and 15. Remove dc voltmeter. Reinstall A8 Circuit board. This completes the check.

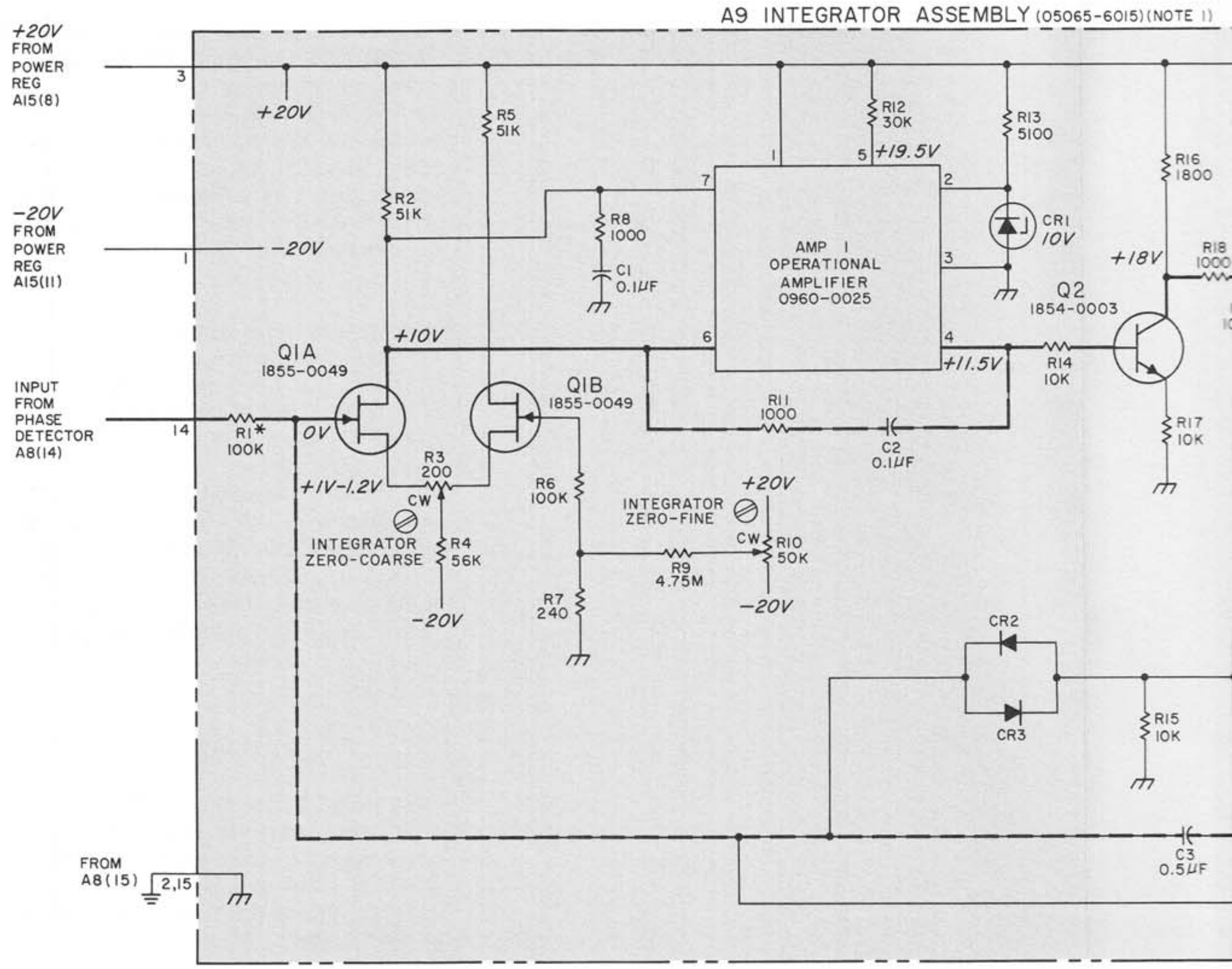
ASSEMBLY REPAIR AND REPLACEMENT

After repair or replacement of A9 Assembly, A9R3 and A9R10 should be adjusted as described in Operational Checks a, b, and c.

Figure 8-19
A9 INTEGRATOR ASSEMBLY

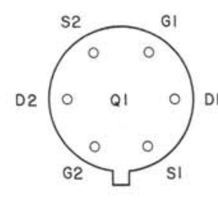
(See Page 8-49)

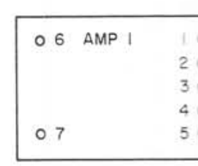

SERIES 820
R25
C24
CR10
R22
R23
R20
C4
R19
CR7
CR6
R12
Q3
R17
CR1
R18
Q2
R16
R13
R14
1
8
15
AMP 1
C2
C3
600 VDC
C1
R10
CR2
CR3
R1
R15
R21
CR4
CR5
CR8
CR9
Q1
R9
R4
R7
R6
R3

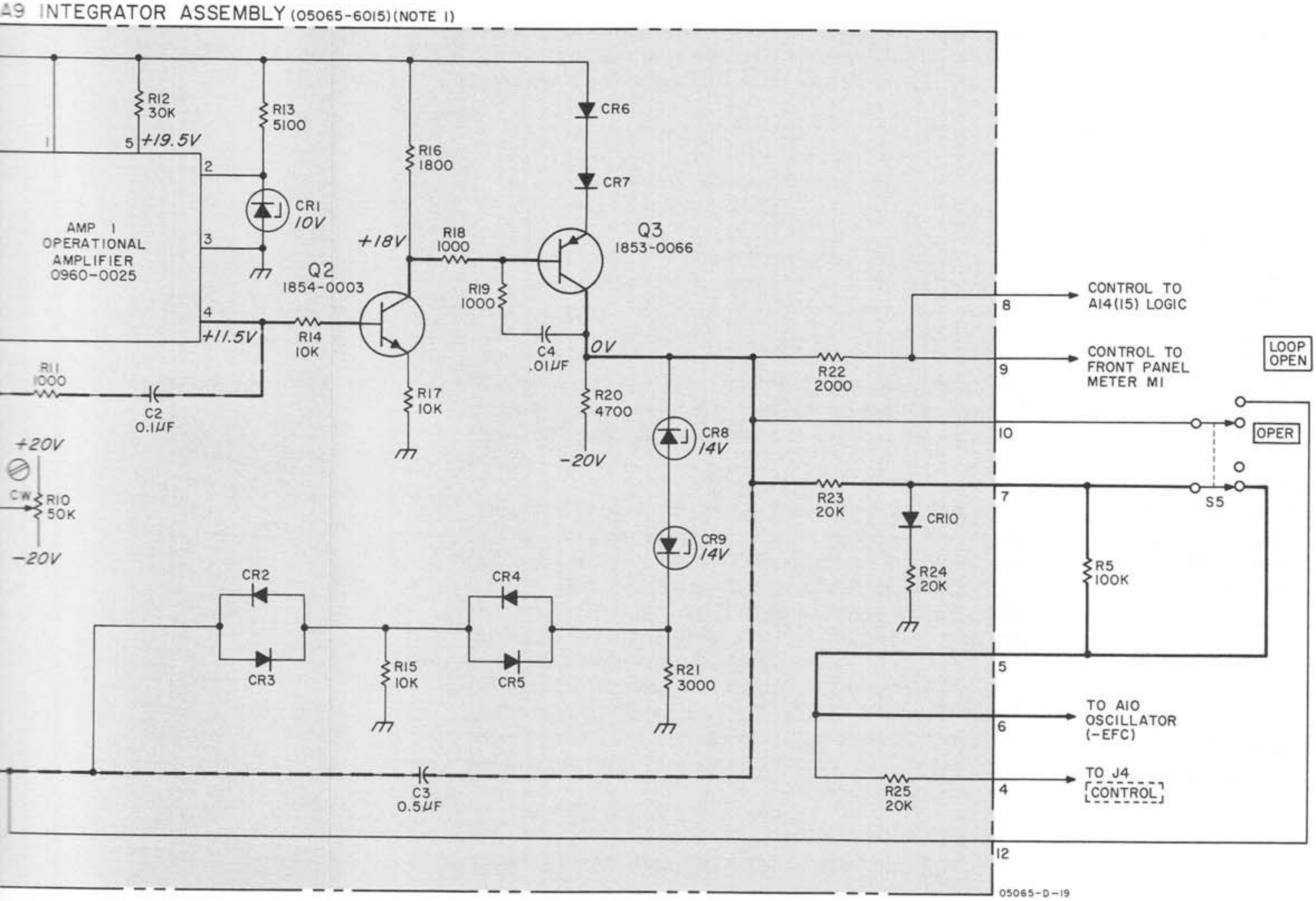


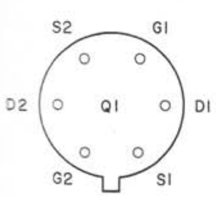
NOTES

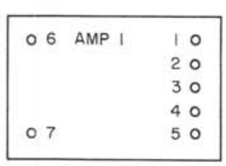
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN
4. DC VOLTAGES WITH FUNCTION SWITCH AT LOOP END.











REFERENCE DESIGNATIONS

NO PREFIX	A9
R5 S5	AMP 1 C1-4 CR1-10 Q1-3 R1-25

Figure 8-19. A9 Integrator Assembly

QUARTZ CRYSTAL OSCILLATOR ASSEMBLY A10 THEORY

GENERAL

The voltage controlled 5 MHz signal is generated by the circuits in Quartz Oscillator Assembly A10. This assembly is composed of 4 major sections:

a. Temperature control circuits.
b. 5 MHz quartz oscillator circuits.
c. Automatic gain control circuits.
d. Power amplifier circuits.

The quartz oscillator generates the 5 MHz signal. The AGC amplifier provides feedback to stabilize oscillator crystal current. Power amplifier circuits and a crystal filter isolate the quartz oscillator from external variations and supply the buffered 5 MHz to Frequency Divider Assembly A6 and Multiplier Assembly A3. Oven control circuits maintain the factory set temperature through proportional control of the internal heater.

The oven temperature is set at the factory to operate the crystal at a temperature where changes in crystal temperature have the smallest effect on oscillator frequency. Placing the quartz oscillator and AGC components inside the oven further improves the oscillator temperature-vs-frequency stability. Shielding and decoupling networks in all leads, except the 5 MHz output, reduce the Radio Frequency Interference radiated or received by the oscillator assembly. The assembly is sealed at the factory; the only adjustments accessible are the Oscillator Frequency FINE knob adjustment, the Oscillator Frequency COARSE screwdriver adjustment, and the Filter crystal adjustment.

TEMPERATURE CONTROL CIRCUITS

PROPORTIONAL CONTROL. Two heaters maintain oven temperature: HR1, which is proportionally controlled to provide continuous oven temperature control; and HR2, which is thermostatically controlled, and provides fast warm-up. The heater current in a proportional control circuit is a continuous function of oven temperature. The heater current in a thermostat control circuit is either "on" or "off", depending on oven temperature setting. Both control circuits contain a thermal fuse to prevent damage to components within the oven, if the assembly overheats.

NOTE

Reference designators in the following paragraphs are abbreviated; for complete reference designators, add prefix "A10" to reference designators used.

PROPORTIONAL TEMPERATURE CONTROL CIRCUITS
Ac Controller A1 is a Wien bridge oscillator with emitter follower and detector providing a dc signal voltage, proportional to oven temperature, for the dc controller. The Wien bridge oscillator frequency (about 3 kHz) is determined by a phase-shifting network in the bridge A1R1, A1R2, A1C1, and A1C2.

The oscillator amplitude is determined by the degenerative feedback through A1R3, A1R4, and RT1 (inside the oven). Since thermistor RT1 is within the oven, Wien bridge coscillator output level is determined by the oven temperature. The thermistor has a negative temperature coefficient so a decrease in oven temperature causes thermistor resistance to increase, increasing oscillator amplitude. Diodes A1CR1, A1CR2, and capacitor A1C10 translate this to a negative dc level applied to the dc controller circuit in A3.

Dc Controller A3Q2, A3Q3, A3Q4, and associated components receives the dc signal (proportional to Wien bridge oscillator amplitude) from ac controller circuits and controls current through HR1. The HR1 heater current is controlled by A3Q4 which is driven through A3Q3 by amplifier A3Q2. Diodes A3CR1 and A3CR2 develop 1.2 volts. The voltage across A3R8 depends on heater current through it, and is added to the voltage across the diodes. This forms a degenerative bias signal for A3Q2. Thus, an increase in current through A3R8 increases A3Q2 current, decreases A3Q4 current and decreases current through A3R8 and HR1.

5 MHz OSCILLATOR AND AGC CIRCUITS

GENERAL. The 5 MHz signal is generated by an electrically controlled quartz crystal oscillator within the oven. An AGC circuit, also in the oven, provides some amplification for the 5 MHz signal and AGC feedback to prevent mechanical vibrations from causing crystal damage. The oscillator frequency is coarse tuned by A2A1C7 which is connected to the front panel Oscillator Frequency COARSE adjustment knob and fine tuned by R3 (front panel Oscillator Frequency FINE adjustment). The only other adjustment that can be performed in the field is the 5 MHz Filter adjustment, A3C10. For access to A3C10, A10 Assembly must be detached from the main chassis. In operation, with the FUNCTION switch at OPER, the oscillator frequency is electrically tuned by the dc error signal from A9 Integrator Amplifier Assembly. This dc error signal connects through A10J1, marked (-EFC) to frequency-controlling Varactor A1A1CR1 to correct the 5 MHz output frequency.

In the oscillator circuit, oscillator stage A1A1Q1 drives resonant circuit A2A1L2, A2A1C6, A2A1C7, A2A1C9, and A2A1CR1. Oscillator feedback is through A1A1C10, A2A1C11, A2A1C12, and A2A1L3 to A2A1Q1 base. Capacitor A2A1C8 serves to bypass A2A1Q1 emitter resistance, A2A1R2. Bias control for oscillator stage A2A1Q1 is provided by the AGC circuit in A2A2 subassembly; as the oscillator output level increases, the AGC circuit decreases A2A1Q1 bias, and decreases oscillator output amplitude.

'aractor A2A1CR1 capacitance decreases as the biasing oltage applied from A9 Assembly through J1 (-EFC) increases positively producing an oscillator frequency icrease. In this manner, oscillator frequency is corected by the dc error voltage to maintain frequency stability with respect to the Rb^{87} resonance. The other input to Varactor A2A1CR1 is the FINE Oscillator Freuency input through J2 (+EFC) from the front-panel INE knob. This control is normally used only for testing and with the instrument operating, is set at 250.

he A2A2 AGC Assembly contains two tuned 5 MHz amplifiers, the AGC circuit, and the 6 and 15 volt power supplies. The +6 volt supply is used as A2A1Q1 colctor supply and as A2A2Q1 and A2A2Q2 bias supply. he +15 volt supply is the reference voltage for R3, the front panel Oscillator Frequency FINE adjustment.

he open-loop gain of tuned amplifier A2A2Q1 is adisted by A2A2R3; the closed-loop gain of A2A2Q1 an A2A2Q2 is determined by feedback resistor A2A2R9. A2A2C5 tunes A2A2Q1 collector resonance. Second ined amplifier stage A2A2Q2 provides output power t 5 MHz to A10A3. One secondary winding from output transformer A2A2T2 provides a feedback signal that in phase with the input signal at A2A2Q1 base; this gnal is fed back to A2A2Q1 emitter through A2A2R9 or gain stabilization of the amplifier pairs; to A2A2Q2 base through A2A2C3 for neutralization; and through 2A2C13 to AGC detecting diodes A2A2CR3 and 2A2CR4. A2A2C11 tunes A2A2T2 for resonance.

Diodes A2A2CR3 and A2A2CR4 provide a dc voltage oportional to the 5 MHz output voltage level this voltje is algebraically added to the bias voltage established by A2A2R11 and AGC gain adjustment A2A2R12. The resultant voltage is fed back to the base A2A1Q1 oscillator stage for bias control to regulate scillator drive level to the quartz crystal.

OA3 POWER AMPLIFIER

The A10A3 assembly contains the 5 MHz output amplifiers and the dc controller circuit which supplies dc rrent for the oscillator oven heater. For a discussion the dc controller, see "Proportional Temperature Control Circuit" at the beginning of this section.

MHz from A2A2 couples through A3C1 to buffer amplifier A3Q1. Selected resistor A3R9 sets A3Q1 gain for the correct ouput at J4 (factory adjustment). This ige feeds adjustable crystal filter network of A3Y1 E12, A3C9, 5 MHz crystal filter adjustment A3C10, A3C11, A3C6, and A3C8. Capacitor A3C6 and A3C8 provide ac voltage division for the 5 MHz output to the Frequency Divider Assembly.

Emitter follower A3Q5 couples the filter network to output amplifier A3Q6. The gain of A3Q6 stage is adjusted A3R19 and collector resonance is tuned with A3C12. utput transformer A3T1 feeds the A3 Multiplier Assembly through A3J3.

Supply voltage filtering is supplied by A3L1 and A3C5 for A3Q1 and by A3R11 and A3C15 for A3Q5 and A3Q6. Additional RF decoupling for A3Q1 is supplied by A3R5 and A3C3.

A10 MAINTENANCE

The oscillator assembly is not recommended for field repair. Instrument warranty is void if repair or adjustment is attempted inside the assembly. Adjustments other than those available on instrument front panel will also void the warranty. If it is established that a defective component or circuit trouble exists within the oscillator assembly, contact the nearest Hewlett-Packard Sales and Service Office for shipping instructions (see paragraph 2-10 for packing information).

OPERATIONAL CHECK

The following procedures may be used to determine proper operation and should be used if the assembly is replaced.

CIRCUIT CHECKS. The following circuit checks involve checking oscillator inputs and outputs.

a. Set instrument to normal operation with front panel MODE switch set to LOOP OPEN.

b. Disconnect the +20 red wire from the oscillator assembly. Connect a high impedance dc voltmeter positive lead (+) to the disconnected red wire. Connect comman (-) voltmeter lead to instrument chassis. Voltmeter should indicate +20 V. Disconnect voltmeter and connect red wire back to +20 terminal on oscillator assembly.

c. Disconnect the +24 white-red-blue wire from oscillator assembly. Connect a high impedance dc voltmeter positive lead (+) to the disconnected white-red-blue wire. Connect common (-) voltmeter lead to instrument chassis. Voltmeter should indicate between +22 and +33 volts. Disconnect voltmeter and connect white-red-blue wire back to +24 terminal on oscillator assembly.

d. Connect high impedance dc voltmeter to wht-orn wire on OSC FREQUENCY $X10^{-10}$ control. Connect common (-) lead to chassis ground. Voltmeter should indicate between +14 and +16 volts. Disconnect voltmeter.

e. Connect dc voltmeter to OSC OVEN pin on Terminal Board Assembly A17(5). Connect common (-) lead to chassis ground. Voltmeter should indicate about +16 volts. Disconnect voltmeter.

f. Connect an oscilloscope vertical channel through a 50-ohm feedthru to A10P3. Oscilloscope display should be 5 MHz, 3 V peak-to-peak. Remove oscilloscope and replace A10P3.

g. Connect oscilloscope vertical channel through a 50-ohm feedthru to A10P4. Oscilloscope display should be 5 MHz, .2 V peak-to-peak. Remove oscilloscope and reconnect A10P4.

h. Set CIRCUIT CHECK switch to 2ND HARMONIC. Adjust OSC FREQUENCY $X10^{-10}$ control maximum clockwise, maximum counterclockwise, and return to 250. CIRCUIT CHECK meter should track with control movement.

i. Disconnect cable from -EFC on oscillator assembly. Connect dc power supply common lead (-) to -EFC on oscillator assembly. Connect positive lead (+) to chassis ground. Slowly adjust dc power supply to -5 volts. CIRCUIT CHECK meter should track with power supply. Disconnect power supply and reconnect -EFC cable.

j. Set CIRCUIT CHECK switch to OSC OVEN, 5 MHz, SUPPLY, and observe CIRCUIT CHECK meter indication at each position. Meter indications should agree with Table 3-1. This completes the oscillator circuit checks.

OUTPUT VOLTAGE AND WAVEFORMS. In addition to the circuit checks, the following checks can be performed, using equipment listed in Table 5-5. To observe 5 MHz output voltage and waveforms:

a. Terminate rear panel 5 MHz output jack with 50-ohm termination and connect an RMS voltmeter to front panel 5 MHz output jack. Output level should be at least 1 V rms. If it is not, use adapter cable provided with instrument and connect ac voltmeter with 50 load to A10J3 ("1 V"). Signal should be 1 V rms. If this signal level is ok, troubleshoot 5 MHz signal path from A10 oscillator assembly to front (or rear) panel. If signal level is less than 1 V rms at A10J3, realign output crystal filter as described below.

b. Remove 50Ω load and, using the adapter cable connect ac voltmeter to A10J4 ("DIV"). Voltage here should be greater than 60 mV. If output from A10J3 ("1 V") as measured above is 1 V rms and output from A10J4 ("DIV") is less than 60 mV rms A10 assembly is probably defective and should be replaced.

Realignment of Output Crystal Filter.

a. Remove ac and dc power from instrument.

b. On bottom deck unsolder 115 Vac connection to A10 assembly. See adjacent Figure for location of these terminals.

c. Tape the ends of these wires so they cannot short or make contact with the chassis.

d. Remove the 4 screws which secure the A10 assembly to the instrument chassis.

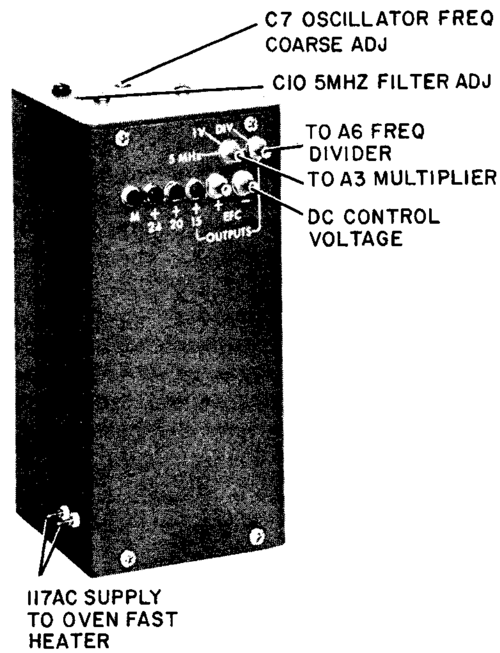
e. Check to see that the wires removed in step 2 are properly insulated.

f. Reconnect ac power, allow instrument to warm up.

g. Connect ac voltmeter with 50Ω load to A10J3.

h. Lift A10 assembly up so that holes on front are accessible. Then, using a non-conductive screwdriver, adjust "5 MHz filter ADJ" (see adjacent Figure) for maximum on meter. This should be 1V rms or greater. If it is not, replace A10 Assembly with restored unit 00105-6034.

i. Remove ac and dc power and reconnect 110 V leads to bottom terminals. Replace protective cover on 110 V terminals, replace 4 hold-down screws, and cable on J3.



NOTE

If Standby Battery Option 002 is installed, remove instrument top cover. Remove ac power and fuse F4 located on instrument deck.

MODULE REPLACEMENT

To remove Oscillator Assembly A10, proceed as follow

a. Remove ALL operating power.

b. Remove bottom cover and disconnect all electrical connections.

c. Remove 4 screws holding oven assembly in place.

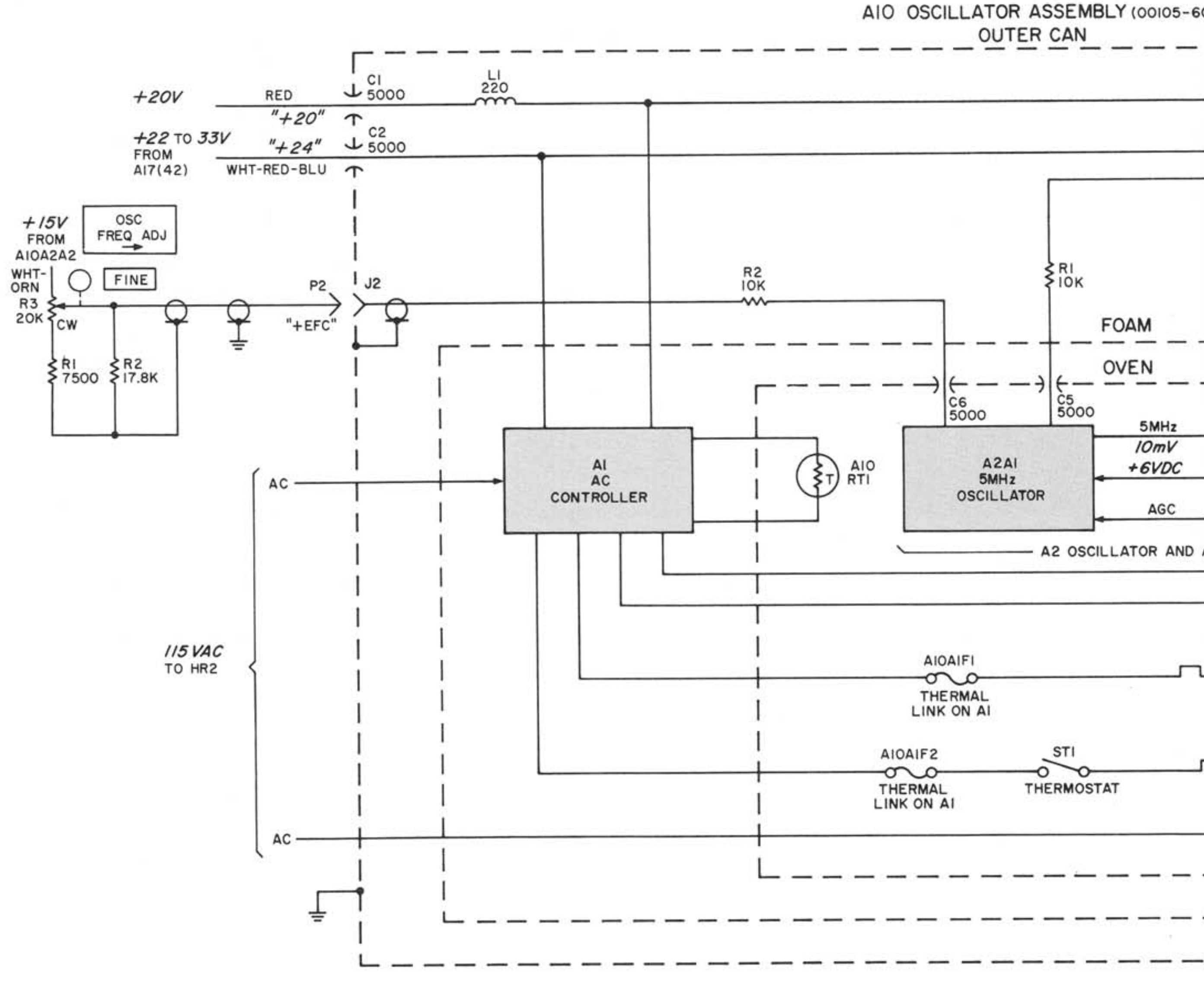
d. Remove oscillator assembly from instrument.

e. Replace oscillator by reversing the above procedure.

f. After replacing the new oscillator assembly, perform turn-on and operational check.

Figure 8-20
A10 OSCILLATOR ASSEMBLY BLOCK DIAGRAM

(See Page 8-53)

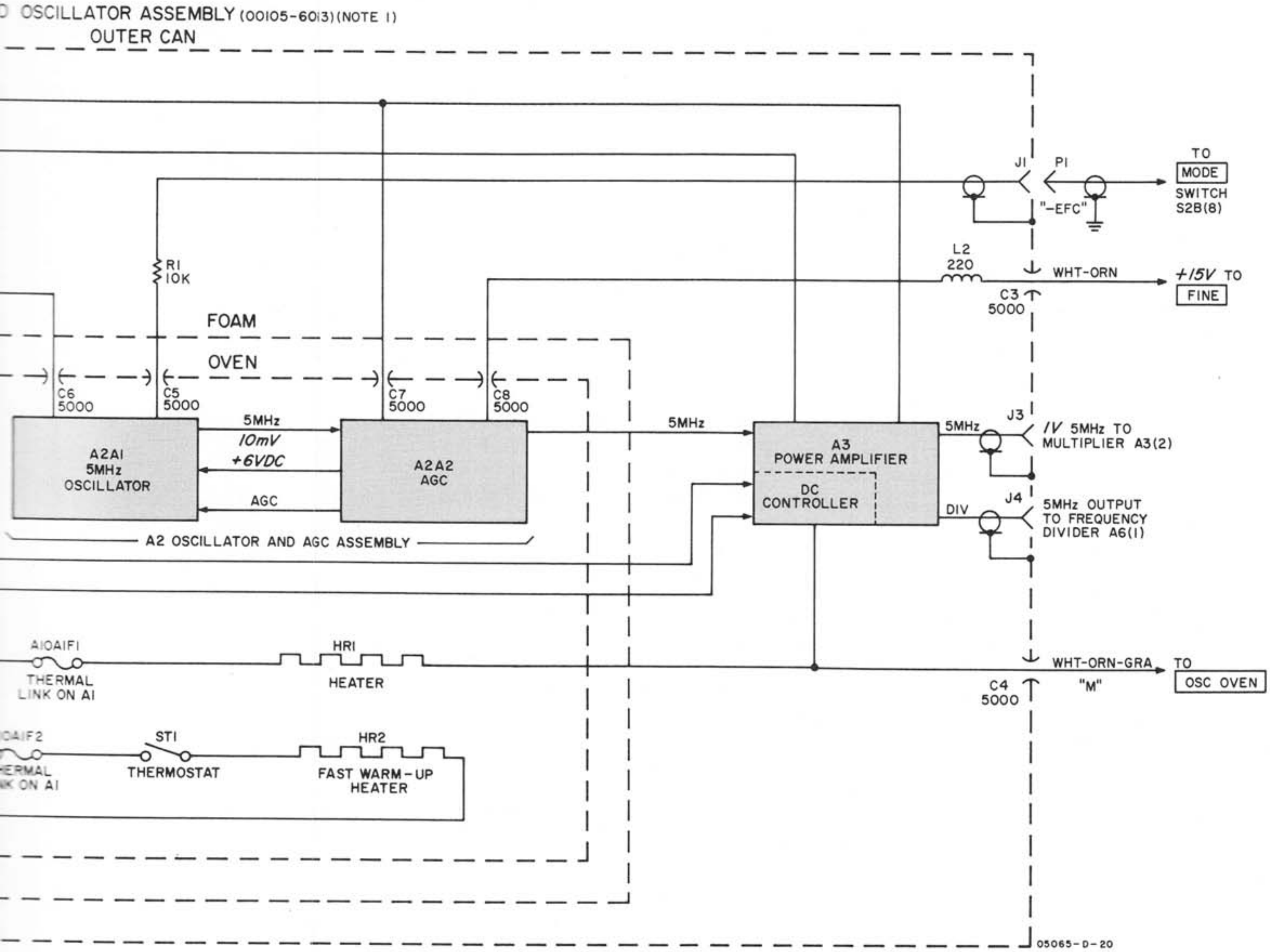


NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

REFERENCE DESIGNATIONS

NO PREFIX	A10	A10A
P1,2 R1-3	C1-8 HR1,2 J1-4 L1,2 R1,2 RT1 ST1	F1,2



REFERENCE DESIGNATIONS

NO PREFIX	A10	A10A1
P1,2 R1-3	C1-8 HR1,2 J1-4 L1,2 R1,2 RT1 ST1	F1,2

Figure 8-20. A10 Oscillator Assembly Block Diagram

TEMPERATURE CONTROLLER A11 THEORY

The A11 Assembly incorporates two temperature controller circuits that work with the sensing and heating elements in A12 RVFR Assembly for temperature control of the Rb^{87} cell, and the Rb^{87} lamp.

The two regulator circuits are nearly identical so discussion will be confined to the upper regulator circuit on A11 schematic (which feeds the cell heater).

Q1 and Q2 comprise a Wein bridge oscillator with emitter follower and detector providing a dc signal voltage representing the required correction for the dc controller section. Oscillator frequency (about 3 kHz) is determined by a phase-shifting network connecting to Q1 base through C8, R1, R3, C1, and C2. Amplitude is determined by the required heater power necessary to maintain proper operating temperature of the cell oven. Information on cell oven temperature is conveyed to the resistive leg of the Wein bridge by A12TR1 in the cell oven. Temperature setting of this heater control circuit is done by selecting A11R5. The cell oven thermistor has a negative temperature coefficient, so a decrease in oven temperature causes thermistor resistance to increase, thereby increasing oscillator amplitude. Diodes CR1 and CR3, and C21 translate oscillator output to a negative dc level applied to Q5.

The negative signal at Q5 base reduces Q5 collector current; which in turn increases Q7 collector current and the heater current output of chassis-mounted Q3. In this manner, heater current is increased to compensate for a temperature drop. When equilibrium is established (oven at required temperature), the Wein bridge is balanced with oscillator amplitude at a level corresponding to the required heater current. Diode CR7 provides temperature stabilization for Q5. Diode CR5 protects Q1 base-to-emitter junction from reverse voltage.

A11 MAINTENANCE

NORMAL OPERATION

The A11 Assembly contains two oven controller circuits. These circuits control the temperature of the spectral lamp and the Rubidium Absorption cell inside the RVFR Assembly A12.

Proper temperatures are maintained by controlling dc current in the oven windings.

The output of the A11 Assembly are at pins 2 and 14. Nominal output voltage is approximately 18 V at these terminals.

OPERATIONAL CHECK

Proper operation of this assembly can be easily checked by (1) placing your hand on the RVFR Assembly and noting that it is warm to the touch and, (2) checking front panel meter indications in the CELL OVEN and LAMP OVEN positions. The meter should read between 15 and 35. (NOTE: These readings will change with ambient temperature.)

TROUBLESHOOTING AND REPAIR

Disconnect ac and dc power before removing A11 Assembly.

ASSEMBLY REPLACEMENT

a. Disconnect ac and dc power (Battery fuse or Option 002).

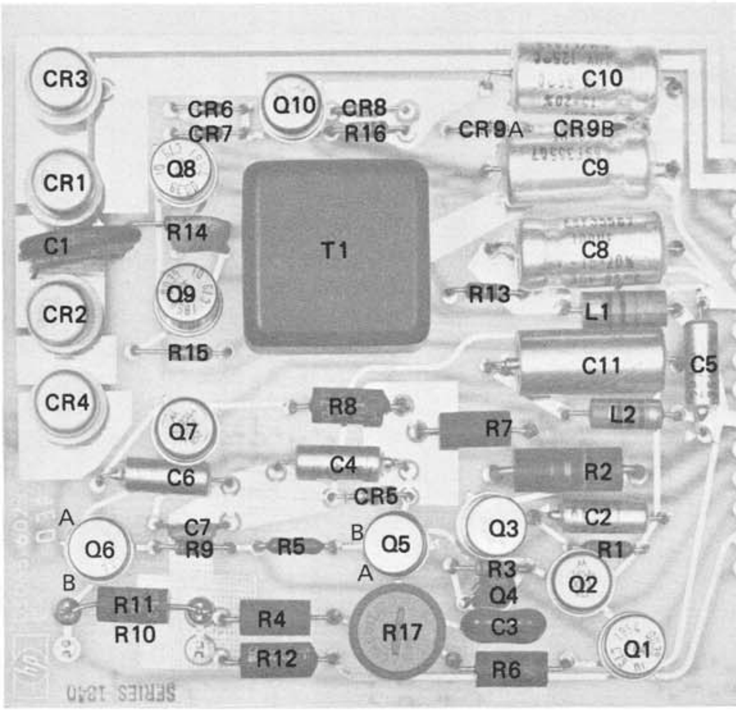
b. Remove A11 Assembly. Remove A11R5 and install it on the new circuit board.

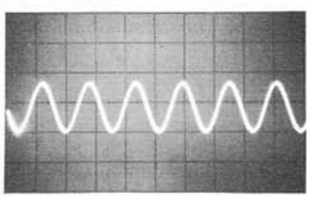
c. Remove A11R6 from the old board and install it on the new one.

d. Install new board and restore power.

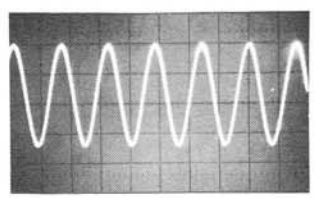
Figure 8-21
A11 RVFR TEMPERATURE CONTROLLER ASSEMBLY

(See Page 8-55)

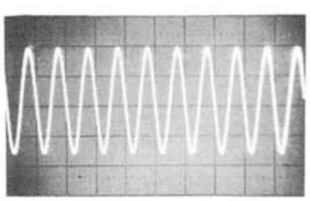




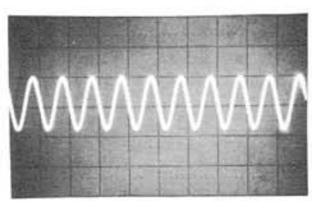
1 .5 V/cm, 1 ms/cm



2 .5 V/cm, 1 ms/cm

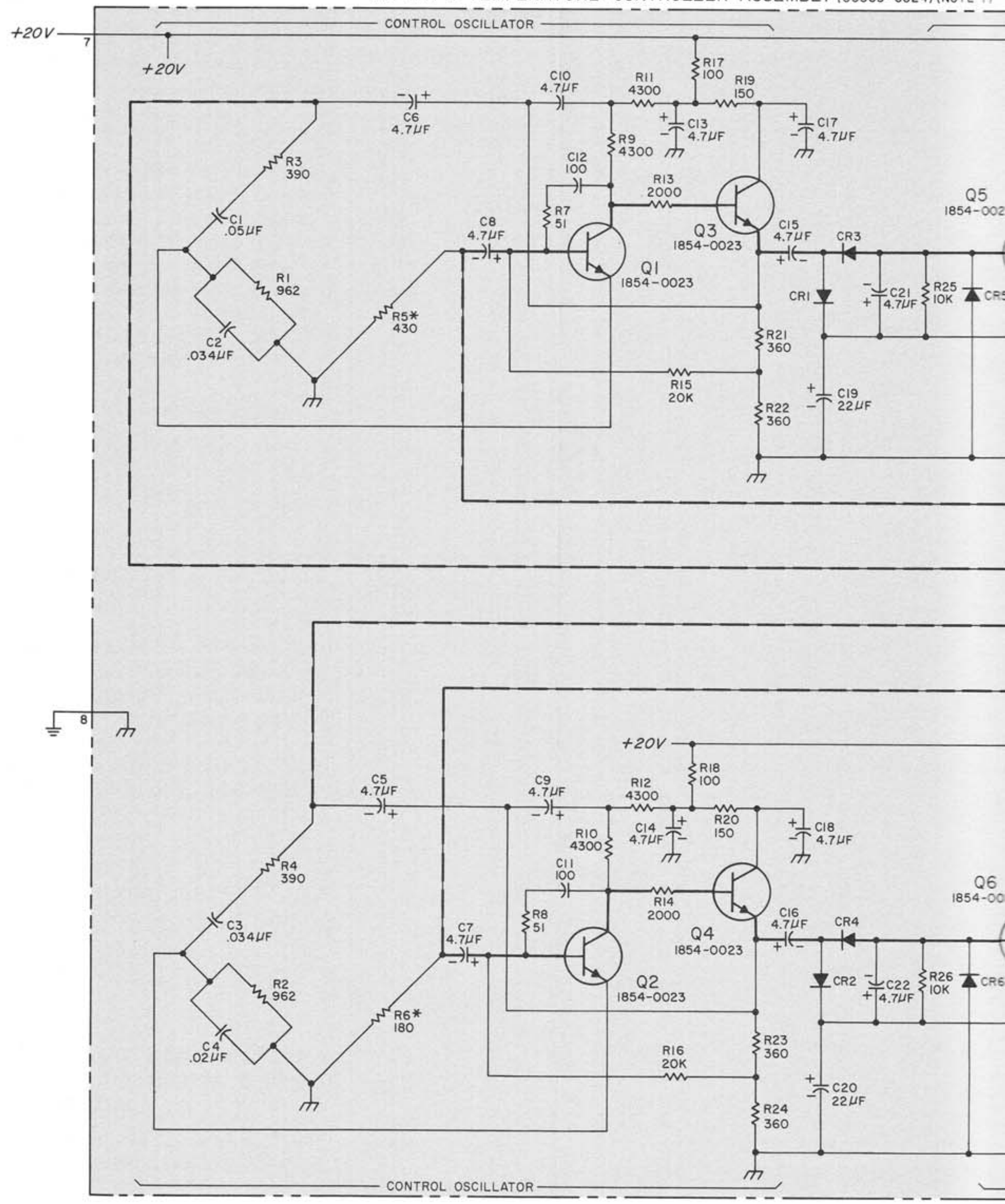


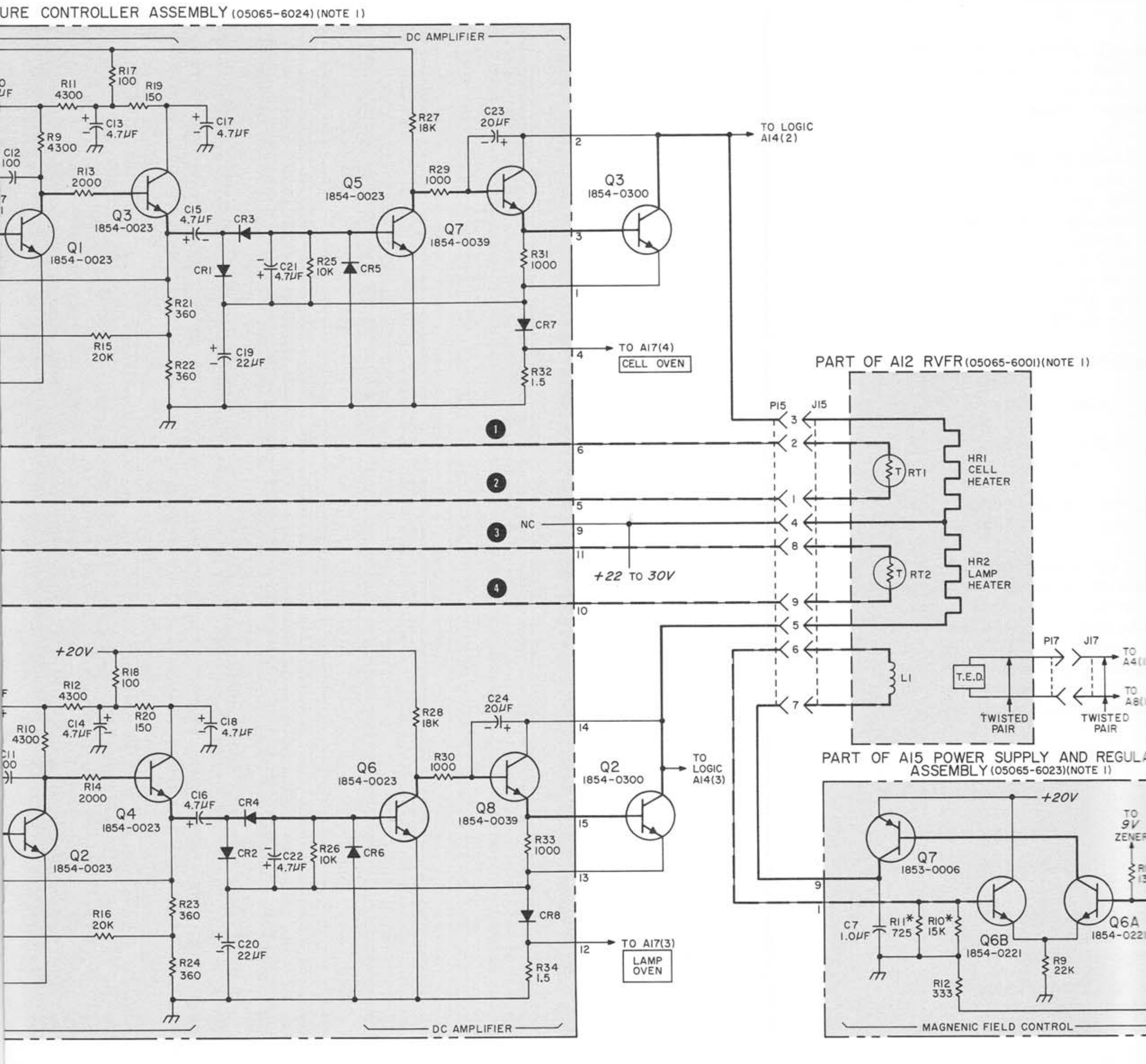
3 .5 V/cm, .1 ms/cm



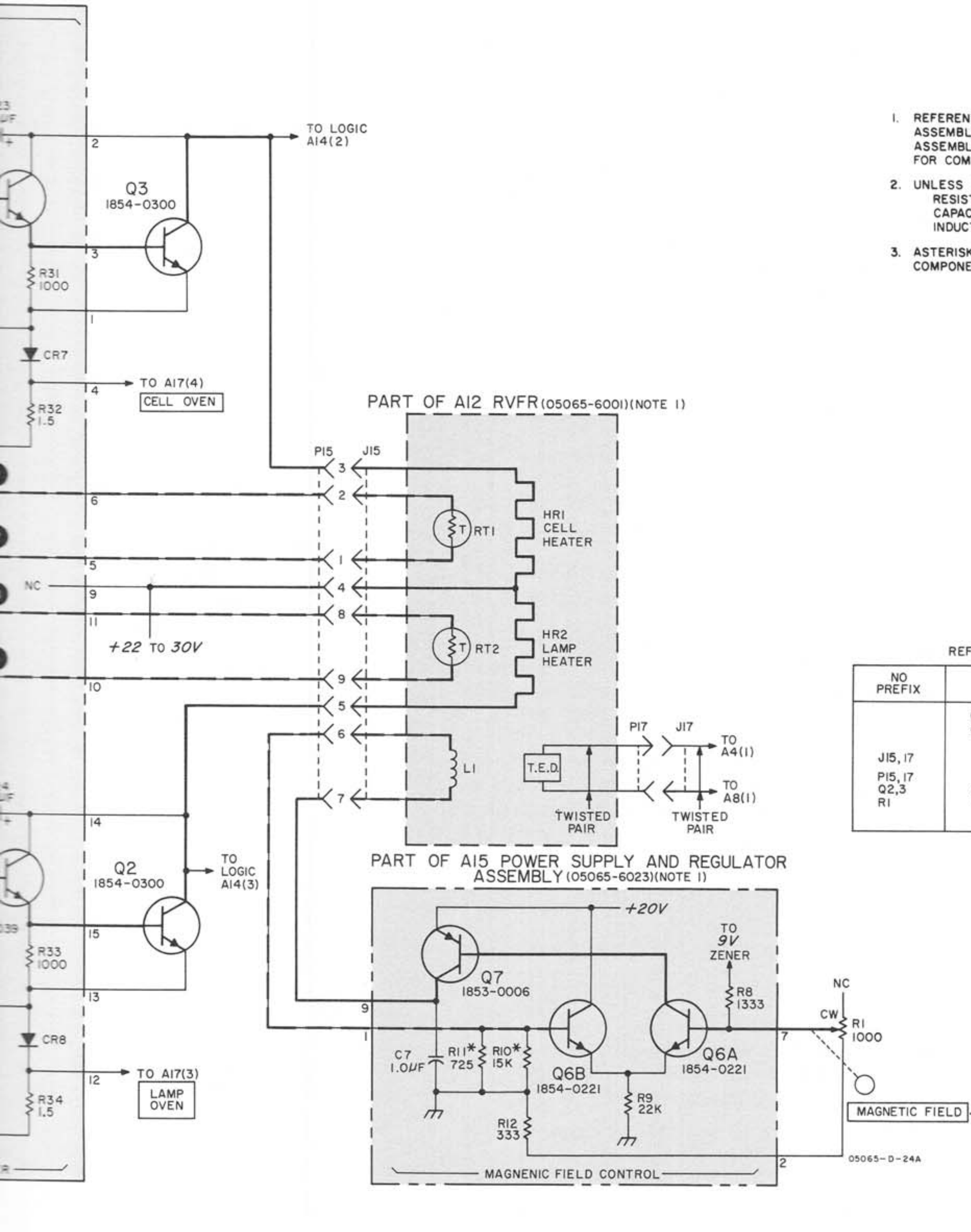
4 .5 V/cm, .1 ms/cm

A11 RVFR TEMPERATURE CONTROLLER ASSEMBLY (05065-6024) (NOTE 1)




URE CONTROLLER ASSEMBLY (05065-6024) (NOTE 1)
DC AMPLIFIER
TO LOGIC A14(2)
TO A17(4)
CELL OVEN
+22 TO 30V
NC
TO LOGIC A14(3)
TO A17(3)
LAMP OVEN
PART OF A12 RVFR (05065-6001)(NOTE 1)
HR1 CELL HEATER
HR2 LAMP HEATER
T.E.D.
TWISTED PAIR
PART OF A15 POWER SUPPLY AND REGULA
ASSEMBLY (05065-6023)(NOTE 1)
+20V
MAGNENIC FIELD CONTROL

Figure



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

REFERENCE DESIGNATIONS

NO PREFIX	A11	A12	A15
J15, 17 P15, 17 Q2,3 R1	C1-24 CR1-8 Q1-8 R1-34	HR1,2 L1 T.E.D. RT1,2	C7 Q6,7 R8-12

Figure 8-21. A11 RVFR Temperature Controller Assembly

RVFR (RUBIDIUM VAPOR FREQUENCY REFERENCE) ASSEMBLY A12 THEORY

The A12 RVFR Assembly is a sealed package which should only be serviced at the factory. To remove, see removal instructions. For a detailed discussion of the frequency standardizing process, see Section 4-1, Theory.

The A12 RVFR Assembly which produces the frequency reference is housed in a triple magnetic shield to prevent frequency shifts by external magnetic fields. Isolation from ambient temperature is provided by two separate ovens which provide regulated temperature for; (1) the Rb^{87} lamp and lamp oscillator and, (2) the Rb^{87} filter cell and the Rb^{87} absorption cell. Oven currents for the LAMP OVEN and CELL OVEN can be monitored with the CIRCUIT CHECK switch.

The main components of A12 Assembly are as follows:

a. The magnetic shields.

b. The temperature ovens each with a temperature sensor and heater.

c. The Rb^{87} lamp and oscillator circuit which produces 90 MHz to excite the lamp.

d. The microwave cavity housing the Rb^{87} absorption cell, the solar cell which detects the light output of the Rb^{87} absorption cell, and the coupler which couples the 6.834685...GHz excitation into the microwave cavity.

e. The step-recovery diode which produces the 114th harmonic of 60 MHz -5.315...MHz (6.834685...GHz) to excite the microwave cavity.

A12 MAINTENANCE

NORMAL OPERATION

a. Inputs:

1) 60 MHz at approximately 1 V or greater from A3 Assembly. Also 5.315...MHz at approximately 20 mV on same cable.

2) Approximately 18 Vdc at J15 (3 and 5) from A11 Temperature Controller Assembly for cell and lamp heaters.

3) Approximately 2½ to 6 mA at J15(6) from A15 Power Regulator Assembly. This current creates the magnetic field inside the RVFR to control its frequency.

b. Outputs: Under normal operation with sufficient RF power applied, the output of A7P1 will be:

1) At resonance, 274 Hz at a signal level of approximately 3 nanoamperes.

2) Slightly off resonance, 137 Hz at a signal level of approximately 5 milliamperes.

3) Completely off resonance, nothing.

4) Dc photo induced current of approximately 50μa.

OPERATIONAL CHECK

a. Because of the extremely low signal level outputs from the RVFR and, because of the specialized nature of the drive signals, the operational check of the RVFR requires that the driving and amplifying circuits associated with the RVFR work properly. Thus, the operational check for the RVFR may include operational checks of several other assemblies.

b. Procedure:

1) Check lamp and cell ovens by placing a hand on the RVFR Assembly. It should be warm to the touch. Also check CIRCUIT CHECK meter in the CELL OVEN and LAMP OVEN positions. Meter should read between 15 and 35 for both positions.

2) Set CIRCUIT CHECK meter to PHOTO I. Meter should read 25 to 50. If it does, go to Step 3. If not proceed as described in the Circuit Checks, Table 5-3.

3) Magnetic field current check. Use clip-on milliammeter such as HP 428B and measure output current at A15(9). It should be between 2½ and 6 mA and be controllable from the front panel MAGNETIC FIELD control.

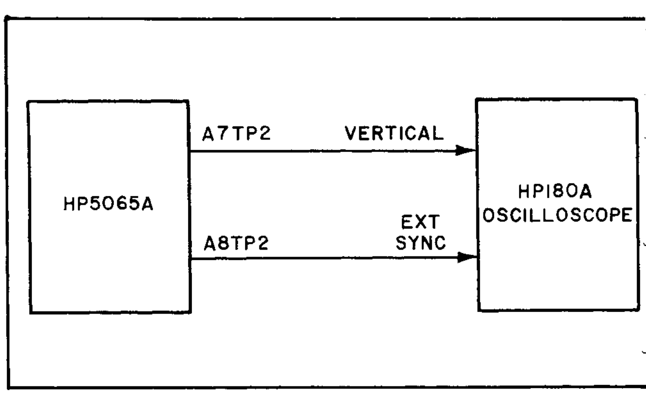
NOTE

Lack of magnetic field current will not affect the signal output of the RVFR. This current controls only the resonant frequency of the RVFR.

c. RVFR signal test:

1) Connect test setup as shown in the following figure:

RVFR Test Setup



2) Set scope sweep to 2 msec/cm and vertical sensitivity for 50 mV/cm. Adjust scope for external sync from signal at A8TP2.

3) Tune OSC FREQ ADJ COARSE for a signal indication on scope. The normal indication as the oscillator is tuned through the RVFR resonance is the appearance of a 137 Hz sine wave; it will increase and then decrease in amplitude, and become 274 Hz at a lower amplitude. It will then become 137 Hz which will again increase and then decrease in amplitude and disappear. If there is no signal go to step 5. Tune the oscillator for maximum undistorted 274 Hz signal, and set CIRCUIT CHECK meter to 2ND HARMONIC. If reading on meter is significantly below that which is normal for the instrument, the instrument should be completely realigned as described in LOOP ALIGNMENT PROCEDURE of Section 5-19.

4) If signal on scope as noted above (or 2ND HARMONIC as noted on front panel meter) is excessively noisy, the signal-to-noise ratio of RVFR should be rechecked as described in Section 5-26 of the instrument alignment procedure. If signal-to-noise ratio is not above 250, the RF alignment should be checked per Section 5-25 of the instrument alignment procedure. The signal-to-noise ratio should then be rechecked. If the signal-to-noise ratio is still less than 250, the RVFR should be replaced. Even with a signal-to-noise ratio of less than 250, the instrument will remain on frequency; however, the short term stability of the instrument will be out of specifications.

5) If no signal was observed in step 3, it indicates trouble in one of several places:

(a) Preamplifier in A7 Assembly not working.

(b) RF output from A3 Assembly low in amplitude or pi-matching network mistuned.

(c) A1 Synthesizer output off frequency or too low in amplitude.

(d) No 137 Hz modulation from A8 Assembly.

(e) Defective RVFR.

6) Items (a) through (d) can be easily checked by referring to the individual maintenance sections. If these circuits are OK, it indicates that the RVFR is probably defective and should be replaced. To check these circuits proceed as follows:

(a) With the instrument set up as shown in the RVFR test setup illustration and oscilloscope setup per preceding step c(2), remove plug A7P1. Touch the center conductor of A7J1 with a small piece of metal such as a piece of solder. A large signal should appear on the scope. This indicates the preamplifier is OK.

(b) Check RF output of A3 Multiplier Assembly by following procedure in the A3 Operational Check.

(c) Check amplitide and frequency of synthesizer output at end of cable at A3P5. Amplitude should be approximately 100 mV and the correct frequency can be found in Table 3-6 after noting Thumbwheel and slide switch settings on the A1 Assembly.

(d) Remove A3P1 and measure the 137 Hz modulation signal present at the end of the cable at A3P1. If signal OK at this point remove and disassembly A3 Assembly. Check diodes A3CR3, 4, 5, and 6. Reconnect cable to A3J1 and +20 V(R). Check signal at CR3 (anode).

7) If all tests to this point are OK, the RVFR is probably defective and should be replaced.

A12 RVFR ASSEMBLY REMOVAL AND REPLACEMENT

a. Disconnect all external power sources including batteries.

b. Remove top and bottom instrument covers.

c. Disconnect RVFR cable from A3J4 on Multiplier Assembly A3.

d. Disconnect RVFR cable from A7J1 on AC Amplifier Assembly A7.

e. Locate the twisted pair of black and red wires from the RVFR Assembly. Disconnect the red wire at socket XA4 pin 1 and the black wire at XA8 pin 1.

NOTE

DO NOT disconnect the diode connected between XA4(1) and XA8(1).

f. Disconnect A12J15 and A12J16 from chassis plugs.

g. Remove four nuts and lockwashers holding the RVFR unit in place and withdraw the assembly from the top of the instrument.

NOTE

When packing for return to the factory, pack carefully for maximum shock cushioning and label shipping package "FRAGILE". If possible, use packing from replacement RVFR unit.

h. Handle replacement RVFR assembly carefully while unpacking and installing. Note two resistors packaged with this Assembly. These are the calibration resistors for the A11 Temperature Regulator Assembly and are required to provide proper operating temperatures for cell and lamp areas of the replacement A12 RVFR Assembly. Install the A12 Assembly in the reverse order of the above removal steps, making sure the four lock washers are in place.

i. Remove the A11 Temperature Regulator circuit board and replace A11R5 and A11R6 with the new R5 and R6 calibration resistors.

j. Install new Power Supply Regulator Assembly supplied with replacement RVFR Assembly.

k. Locate the twisted pair of black and red wires from the RVFR Assembly. Solder the black wire to pin 1 of socket XA8 and the red wire to pin 1 of socket XA4.

l. After the A12 RVFR Assembly has been replaced the instrument should be turned on and warmed up for at least four hours before following the LOOP ALIGNMENT PROCEDURE in paragraphs 5-19 through 5-31.

NOTE

If the A1 synthesizer thumbwheel setting are changed or service is performed on A14, allow 1 minute of recovery time before attempting to place in the continuous operation mode.

BUFFER AMPLIFIER ASSEMBLY A13 THEORY

This assembly has two buffer amplifier circuits which deliver 1 volt (into 50 ohms), 5 MHz outputs. One output goes to A1 Synthesizer Assembly and the other output to front and rear 5 MHz output jacks.

R1 provides a 50-ohm input at J1. Buffer amplifier stage Q2 amplifies the input 5 MHz signal for a 1-volt, 5 MHz output at J3. Buffer Amplifier stages Q1 and Q2 provide a 1-volt, 5 MHz output at J4 for the rear 5 MHz output and at J2 for the front panel 5 MHz output. Additionally, Q3 output is rectified by CR2 and filtered by C11, R17, and C12 for a dc output to the 5 MHz position of the CIRCUIT CHECK meter. Bias voltage for all three amplifying stages is provided by Zener Diode CR1. Selected capacitances C7 and C8 provide tuning for T1 and T2 respectively. The +20 volt supply is decoupled by L1 and C1.

A13 MAINTENANCE

NORMAL OPERATION

a. Input signal is 1V rms.

b. Output at J3 is approximately 3V peak-to-peak into an open circuit.

c. Output at J4 and J2 is 1V rms into a 50 ohm load.

d. Output at C2 is approximately 90 to 120μ a for operation of front panel meter.

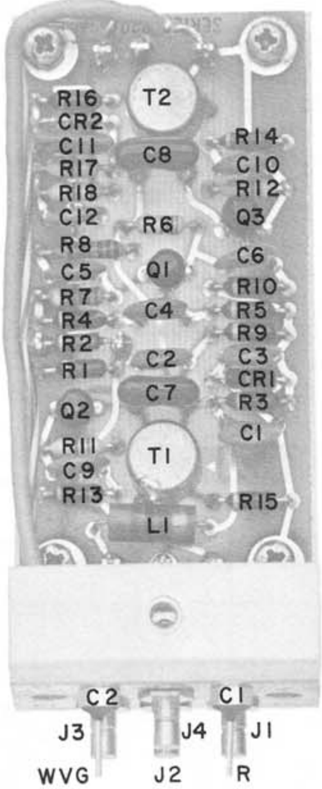
No adjustments are provided.

ASSEMBLY REPLACEMENT

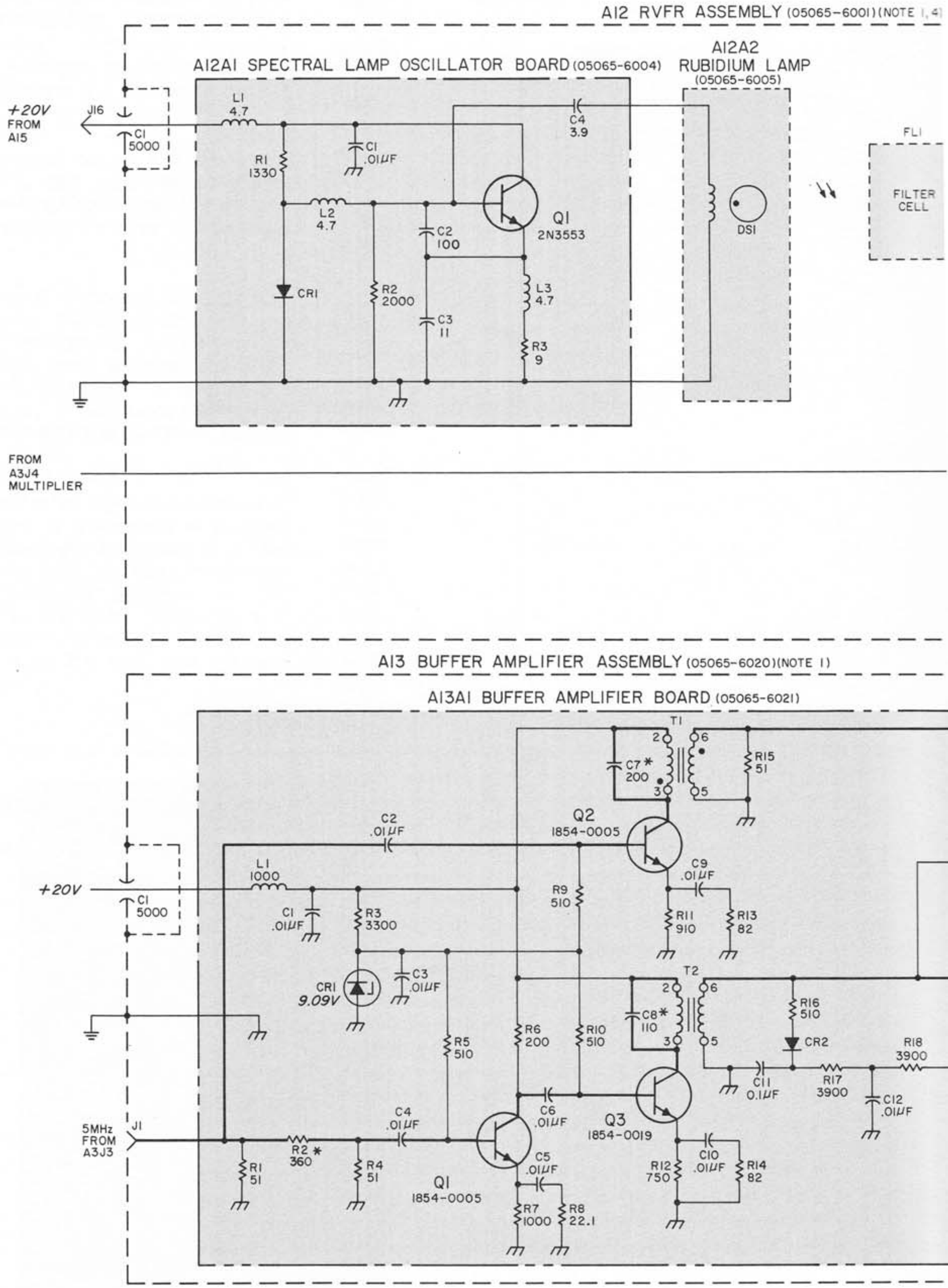
No adjustments are needed after repair or replacement of this assembly.

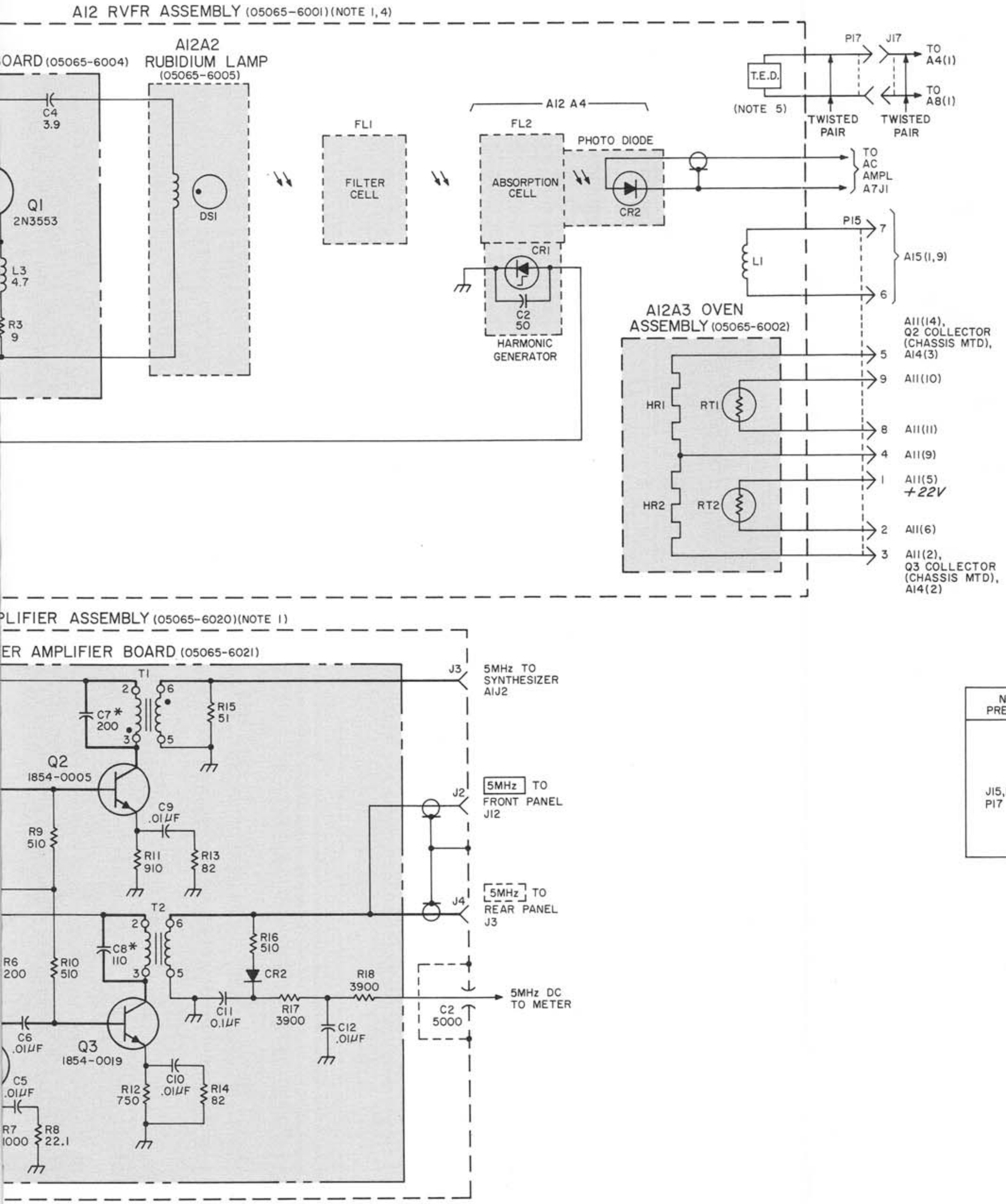
Figure 8-22
A12 RVFR ASSEMBLY AND BUFFER
A13 AMPLIFIER ASSEMBLY

(See Page 8-59)



R16
CR2
C11
R17
R18
C12
R8
C5
R7
R4
R2
R1
Q2
R11
C9
R13
T2
C8
R6
Q1
C4
C2
C7
T1
L1
R14
C10
R12
Q3
C6
R10
R5
R9
C3
CR1
R3
C1
R15
C2
C1
J3
J4
J1
WVG
J2
R

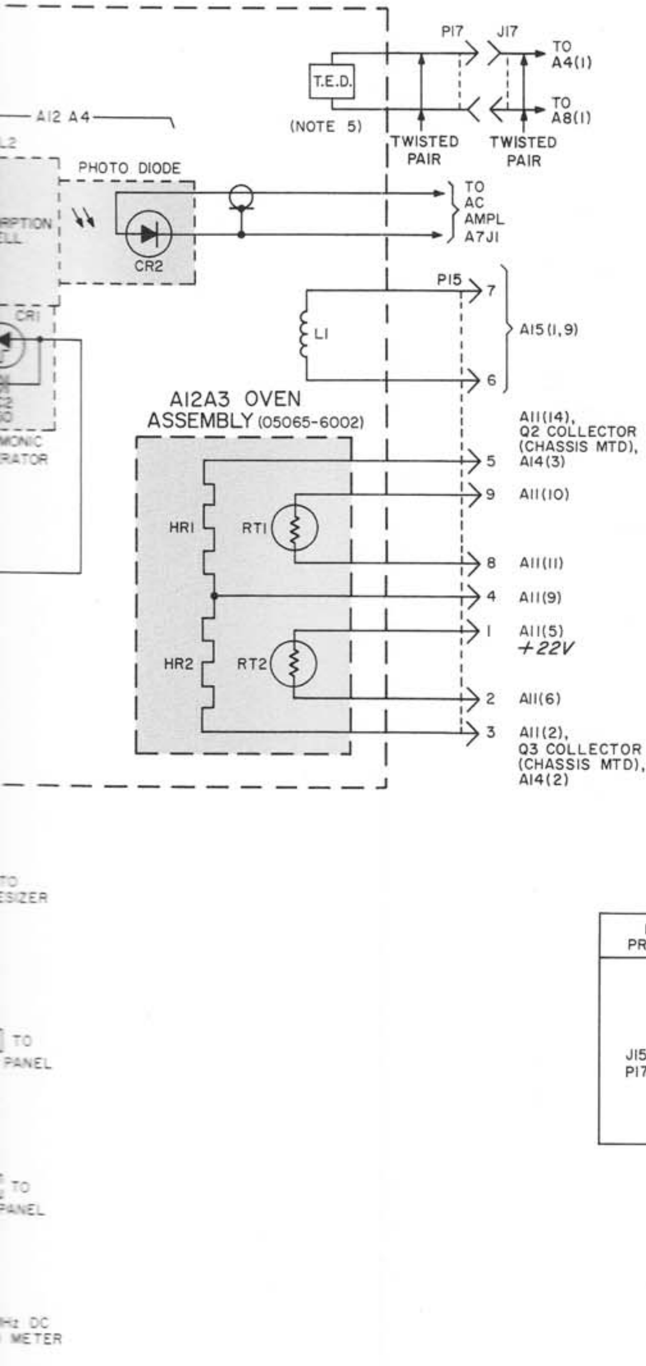

A12 RVFR ASSEMBLY (05065-6001) (NOTE 1, 4)
A12A1 SPECTRAL LAMP OSCILLATOR BOARD (05065-6004)
A12A2
RUBIDIUM LAMP
(05065-6005)
+20V
FROM
A15
J16
C1
5000
L1
4.7
R1
1330
C1
.01μF
L2
4.7
CR1
R2
2000
C2
100
C3
11
Q1
2N3553
L3
4.7
R3
9
C4
3.9
DS1
FL1
FILTER
CELL
FROM
A3J4
MULTIPLIER
A13 BUFFER AMPLIFIER ASSEMBLY (05065-6020) (NOTE 1)
A13A1 BUFFER AMPLIFIER BOARD (05065-6021)
+20V
C1
5000
L1
1000
C1
.01μF
R3
3300
CR1
9.09V
C3
.01μF
C2
.01μF
Q2
1854-0005
T1
C7 *
200
R15
51
C9
.01μF
R9
510
R11
910
R13
82
T2
C8 *
110
R16
510
CR2
R18
3900
R17
3900
C11
0.1μF
C12
.01μF
R5
510
R6
200
R10
510
C6
.01μF
Q3
1854-0019
5MHz
FROM
A3J3
J1
R1
51
R2 *
360
R4
51
C4
.01μF
Q1
1854-0005
C5
.01μF
R7
1000
R8
22.1
R12
750
C10
.01μF
R14
82



REF

NO PREFIX	A12	A12A1
	C1	C1-4 CR1
	FL1	
J15,17 P17	J2 L1 T.E.D.	L1-3 Q1 R1-3

DELETED:
J2



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN
4. NOT FIELD REPAIRABLE.
5. T.E.D. = THERMO ELECTRIC DEVICE

REFERENCE DESIGNATIONS

NO PREFIX	A12	A12A1	A12A2	A12A3	A12 A4	A13	A13A1
J15,17 P17	C1 FL1 J2 L1 T.E.D.	C1-4 CR1 L1-3 Q1 R1-3	DS1	HR1,2 RT1,2	C2 CR1,2 FL2	C1,2 J1-4	C1-12 CR1-2 L1 Q1-3 R1-18 T1,2

DELETED:
J2

05065-D-25A

Figure 8-22. A12 RVFR Assembly and Buffer A13 Amplifier Assembly

LOGIC ASSEMBLY A14 THEORY

Logic Assembly A14 monitors various circuits and controls front panel CONTINUOUS OPERATION and INTEGRATOR LIMIT lights. These two front-panel lights give a constant indication of instrument operation. A14 Functional Diagram is a diagram of the A14 Logic Circuits.

The separate logic functions fed to A14 are listed, together with the normal and abnormal conditions which control the CONTINUOUS OPERATION and INTEGRATOR LIMIT lights, in the table of A14 logic inputs.

With a normal "on frequency" condition, CR13 input is "H" with CR13 conducting, Q18 conducting, and the CONTINUOUS OPERATION light on. At this time, all stages connecting to CR13 input are nonconducting. When Q4, Q14, or Q7 conducts in response to a "no go" logic input, CR13 input goes "L" and stops conducting, Q18 turns off and the CONTINUOUS OPERATION light goes out.

Q14 is noninverting so that a "H" input in normal operation corresponds to a "H" at Q14 output which connects to CR13. Correspondingly, Q15 input is "L" for normal operation. Summarizing, the conducting transistors for a normal "on frequency" condition are: Q5, Q9, Q6, Q8, Q10, Q12, Q3, and Q18; CR13 also conducts. Nonconducting transistors for a normal "on frequency" condition are: Q16, Q4, Q15, Q14, Q2, and Q7.

The cell oven and lamp oven inputs are the voltages at the inputs to the cell and lamp oven heaters. Since these heaters are connected to the dc supply voltage (+22 to 30 volts) these inputs go "L" with an increase in heater current and "H' with no heater current.

With a cell oven "no heater" condition, the cell oven input is near zero volts and Q5 is turned off inpressing an "H" signal on Q15 and the CONTINUOUS OPERATION light is turned off.

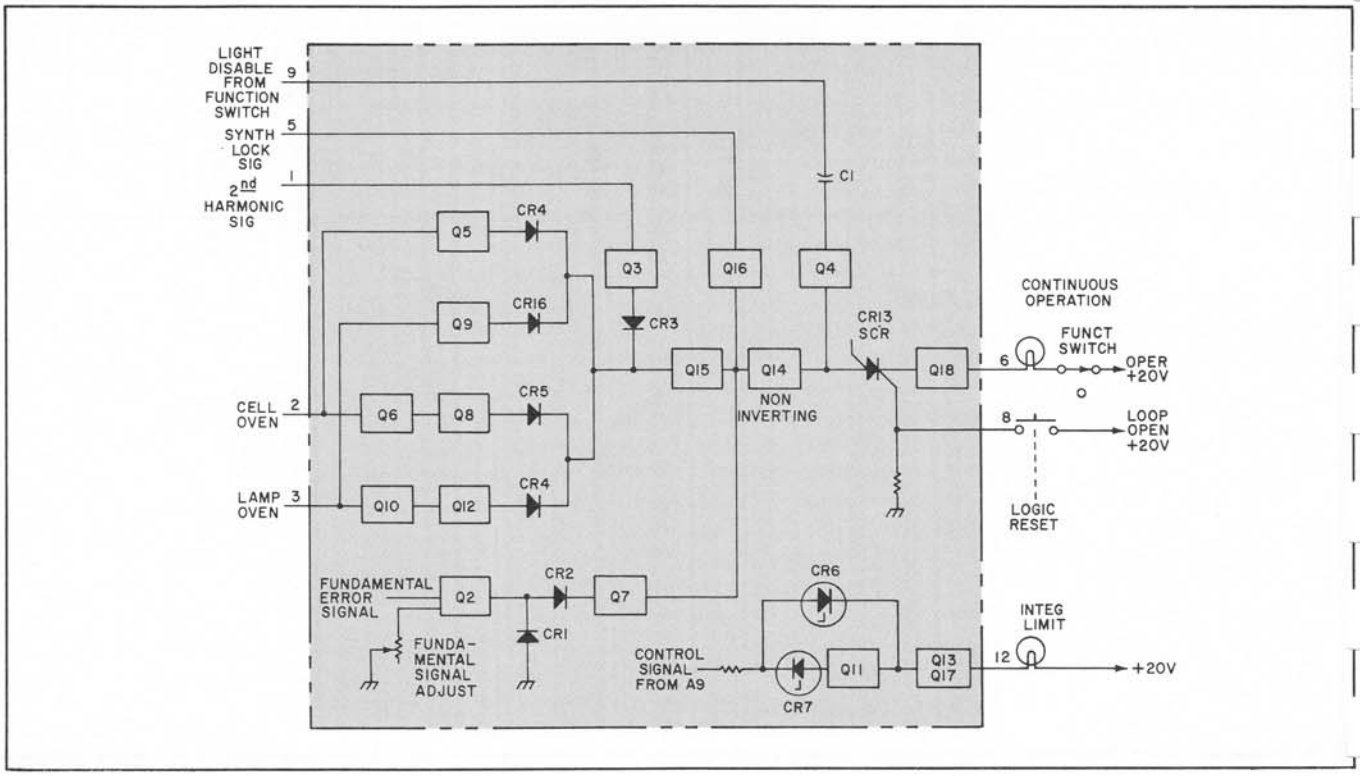
The lamp oven input works in a similar manner as the preceeding for a "no-heater" condition with Q10 and Q12; and for an "over-heat" condition with Q9.

The 2nd Harmonic input to Q3 is a positive dc voltage when "on frequency" resulting in a normal "L" input to Q15. When the system is not operating correctly and 2nd harmonic drops out, Q3 input is "L" and a resulting "H" at Q15 input turns off the CONTINUOUS OPERATION lamp.

The Synthesizer lock signal input is only present when there is no phase lock in the Synthesizer Assembly and consequently the synthesizer output is "off" frequency. The Synthesizer "no go" input is "H" which causes Q16 to conduct, delivering a "L" input to Q14 and the CONTINUOUS OPERATION light is turned off.

The light disable function that comes from the FUNCTION switch is developed when the FUNCTION switch is placed in OPER connecting +20 volts to C2. The result is a short-duration positive pulse at Q4 input. Q4

A14 Functional Diagram



output is a negative spike which turns off CR13. If all inputs to A14 are "go" at this time, the LOGIC RESET pushbutton will cause CR13 to conduct when it is depressed. Q18 will then conduct turning on the CONTINUOUS OPERATION light. This circuit insures that the CONTINUOUS OPERATION light will not come on automatically when the FUNCTION switch is set at OPER.

At the fundmental error input, there is no 137 Hz signal when "on frequency". 137 Hz appears for an "off frequency" condition. After amplification by Q2, the 137 Hz input is rectified by CR1 and CR2 to provide an "H" input to Q7 which delivers a "L" input to CR13 to cut it off, thereby disabling the CONTINUOUS OPERATION light.

A14 MAINTENANCE

NORMAL OPERATION

The A14 Assembly monitors several voltages throughout the 5065A and either extinguishes the CONTINUOUS OPERATION light or enables the INTEGRATOR LIMIT light if these voltages should deviate from prescribed limits.

Loss of the continuous operation light means that the 5065A is probably off frequency. The light will not come back on by itself; the logic reset button must be pushed.

NOTE

If the A1 synthesizer thumbwheel setting are changed or service is performed on A14, allow 1 minute of recovery time before attempting to place in the continuous operation mode.

The table below summarizes the normal and abnormal voltages that operate the A14 Assembly.

OPERATIONAL CHECK

a. Remove ac and dc power.

b. Remove A11 Assembly and mount on extender board.

c. Reapply power and wait a few minutes for instrument to stabilize. Press LOGIC RESET button. Continuous OPERATION light will come on.

d. Set meter to CELL OVEN.

e. Momentarily short Q5 collector (case) to ground. The meter should fall to zero and the CONTINUOUS OPERATON light will go out.

f. Push logic reset button. Momentarily short Q5 base to ground. Meter reading should increase and CONTINUOUS OPERATION light will go out.

g. Press LOGIC RESET button. Set meter to LAMP OVEN. Momentarily connect Q6 collector (case) to ground. Meter should drop to zero and CONTINUOUS OPERATION light will go out.

h. Press logic reset button. Momentarily connect Q6 base to ground. Meter reading will increase and CONTINUOUS OPERATION light will go out.

i. Remove ac and dc power and replace A11 in its socket. Restore power.

j. Perform checks of Paragraph 5-31(e).

A14 Operating Voltages

Pin No.	Signal Source	Normal Voltage	Voltage Required to Extinguish CONT. OP. Light		INTEGRATOR Limit Light On At
1	2nd Harmonic Signal Level	Approximately 8 Vdc	$<$1.1 Vdc		
2	Cell Oven Voltage	18 Vdc	$<$5 Vdc	1 Vdc Less than Pin 7	
3	Lamp Oven Voltage	15 Vdc	$<$5 Vdc	1 Vdc less than Pin 7	
5	Synthesizer Lock Alarm Circuit	$<$1.5 Vdc	5 Vdc		
9	Function Switch	20 Vdc	20 Vdc + Pulse		
11	137 Hz Error Signal	AC Noise	12 V p-p		
15	Quartz Oscillator Control	-14 to +7 dc			+2.5 Vdc or -5 Vdc

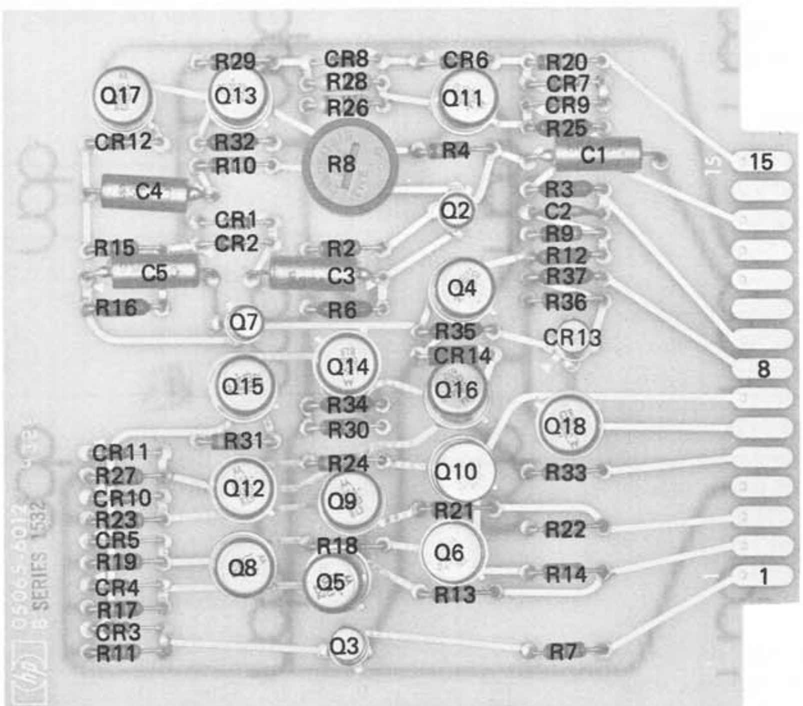
A14 Logic Table

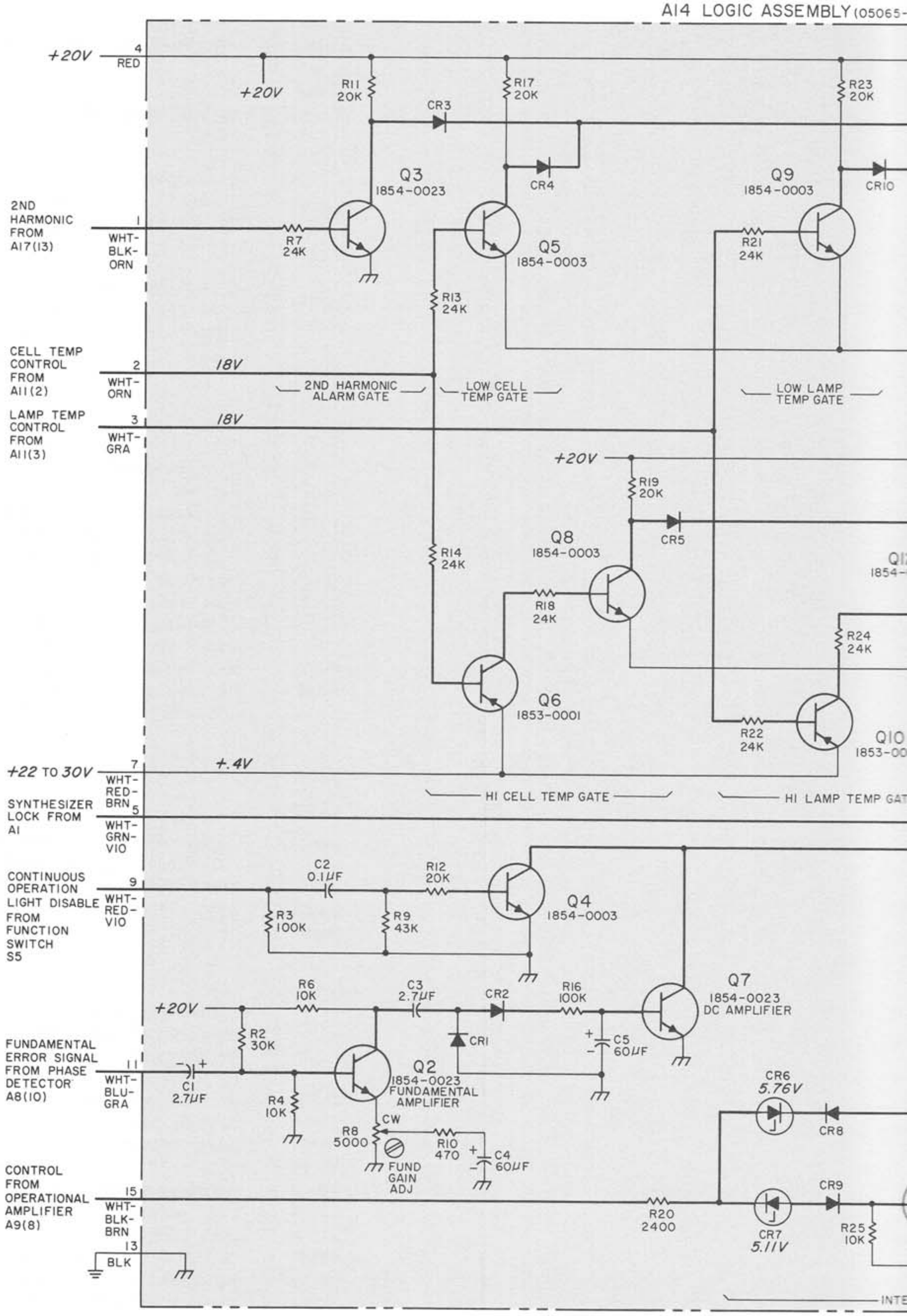
Function	Normal Condition (Continuous Operation Light On)	Abnormal Condition (Causing Continuous Operation Light Off)
Cell Oven (Oven Off Signal)	Positive Voltage Approximately Halfway Between Ground and Dc Supply Voltage	"H"* causing Q8 to cut off and deliver an "H" input to Q15
Cell Oven (Oven Over-Heat Signal)	Same as above	"L"* causing Q5 to cut off and deliver an "H" input to Q15
Lamp Oven (Oven Off Signal)	Same as above	"H"* causing Q12 to cut off and deliver an "H" input to Q15
Lamp Oven (Oven Over-Heat Signal)	Same as above	"L"* causing Q12 to cut off and deliver an "H" input to Q15
2nd Harmonic Signal	"H" when "On Frequency"	"L" for absence of 2nd Harmonic when "off frequency"
Fundamental Error Signal (137 Hz)	"L" for minimum 137 Hz when "ON Frequency"	"H" for large amount of 137 Hz when "off frequency"
Synthesizer Lock Signal	"L" for absence of synthesizer logic input when "On Frequency"	"H" Synthesizer Lock Signal present indicating: (1) No Phase Lock (2) No 5.315...MHz
Light Disable Signal	When +20 volts connects to C2 in the OPER position of the FUNCTION switch, resulting positive spike is inverted by Q4 for a "no-go" negative spike which latches CR13 off and disables the CONTINUOUS OPERATION light until the LOGIC RESET pushbutton is depressed to turn on CR13	

*With respect to normal voltages.

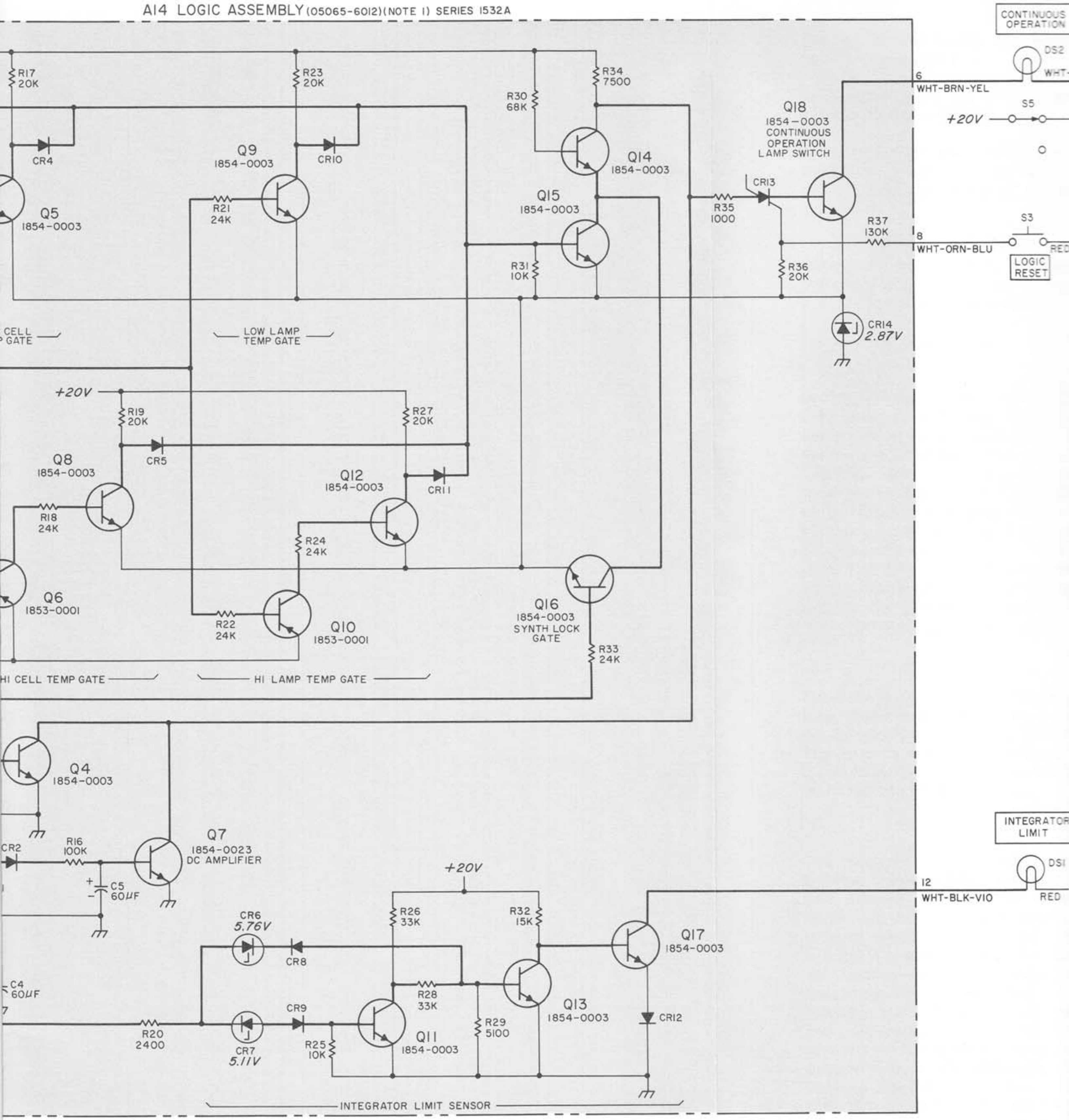
Figure 8-23
A14 LOGIC ASSEMBLY

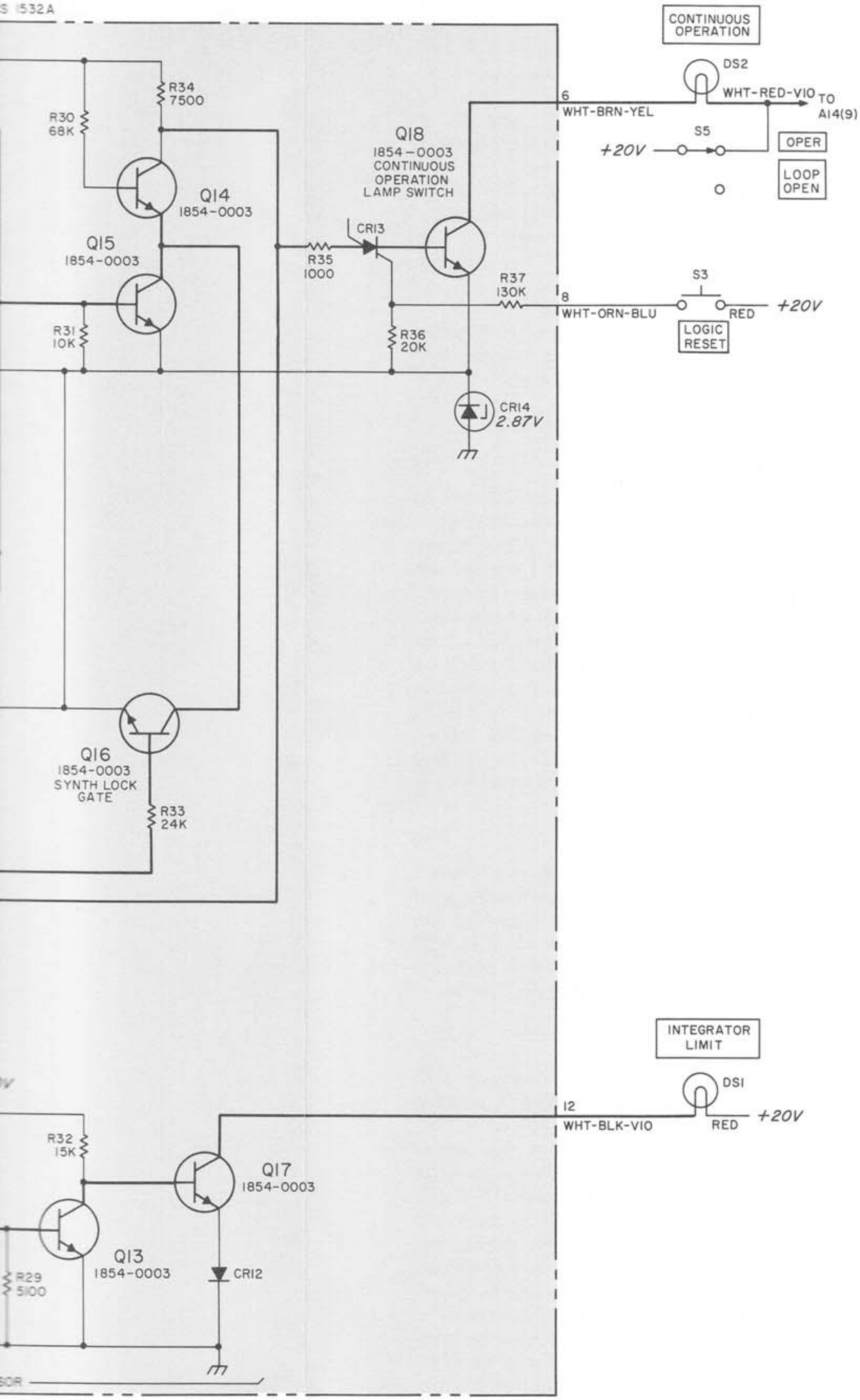
(See Page 8-63)


R29
CR8
R28
R26
CR6
R20
CR7
CR9
R25
Q17
Q13
Q11
CR12
R32
R10
R8
R4
C1
15
C4
CR1
CR2
Q2
R3
C2
R9
R15
C5
R2
C3
R12
R37
Q4
R16
R6
R36
Q7
R35
CR13
CR14
Q14
8
Q15
Q16
R34
R30
Q18
R31
CR11
R24
R27
Q10
R33
Q12
CR10
Q9
R21
R23
R22
CR5
R18
R19
Q8
Q6
CR4
Q5
R14
1
R17
R13
CR3
Q3
R7
R11



A14 LOGIC ASSEMBLY (05065-
+20V
RED
WHT-BLK-ORN
2ND HARMONIC FROM A17(13)
CELL TEMP CONTROL FROM A11(2)
WHT-ORN
LAMP TEMP CONTROL FROM A11(3)
WHT-GRA
18V
Q3 1854-0023
Q5 1854-0003
Q9 1854-0003
Q8 1854-0003
Q6 1853-0001
Q4 1854-0003
Q7 1854-0023 DC AMPLIFIER
Q2 1854-0023 FUNDAMENTAL AMPLIFIER
R11 20K
R17 20K
R23 20K
R7 24K
R13 24K
R21 24K
R19 20K
R14 24K
R18 24K
R24 24K
R22 24K
CR3
CR4
CR10
CR5
2ND HARMONIC ALARM GATE
LOW CELL TEMP GATE
LOW LAMP TEMP GATE
HI CELL TEMP GATE
HI LAMP TEMP GAT
+22 TO 30V
WHT-RED-BRN
+.4V
SYNTHESIZER LOCK FROM A1
WHT-GRN-VIO
CONTINUOUS OPERATION LIGHT DISABLE FROM FUNCTION SWITCH S5
WHT-RED-VIO
C2 0.1µF
R12 20K
R3 100K
R9 43K
R6 10K
C3 2.7µF
CR2
R16 100K
C5 60µF
CR1
R2 30K
FUNDAMENTAL ERROR SIGNAL FROM PHASE DETECTOR A8(10)
WHT-BLU-GRA
C1 2.7µF
R4 10K
R8 5000
CW
R10 470
C4 60µF
FUND GAIN ADJ
CR6 5.76V
CR8
CR9
CR7 5.11V
CONTROL FROM OPERATIONAL AMPLIFIER A9(8)
WHT-BLK-BRN
R20 2400
R25 10K
BLK
INTE


A14 LOGIC ASSEMBLY (05065-6012)(NOTE 1) SERIES 1532A
CONTINUOUS OPERATION
DS2
S5
+20V
S3
LOGIC RESET
INTEGRATOR LIMIT
DS1
RED
WHT-BRN-YEL
WHT-ORN-BLU
WHT-BLK-VIO
R17 20K
R23 20K
R30 68K
R34 7500
CR4
CR10
Q9 1854-0003
Q14 1854-0003
Q18 1854-0003 CONTINUOUS OPERATION LAMP SWITCH
Q5 1854-0003
Q15 1854-0003
R21 24K
CR13
R35 1000
R37 130K
R31 10K
R36 20K
CR14 2.87V
LOW LAMP TEMP GATE
+20V
R19 20K
R27 20K
CR5
Q8 1854-0003
Q12 1854-0003
CR11
R18 24K
R24 24K
Q6 1853-0001
Q16 1854-0003 SYNTH LOCK GATE
R22 24K
Q10 1853-0001
R33 24K
HI CELL TEMP GATE
HI LAMP TEMP GATE
Q4 1854-0003
Q7 1854-0023 DC AMPLIFIER
CR2
R16 100K
C5 60μF
+20V
R26 33K
R32 15K
CR6 5.76V
CR8
Q17 1854-0003
C4 60μF
R28 33K
Q13 1854-0003
CR9
R20 2400
CR7 5.11V
R25 10K
Q11 1854-0003
R29 5100
CR12
INTEGRATOR LIMIT SENSOR



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;

REFERENCE DESIGNATIONS

NO PREFIX	A14
	C1-5
	CR1-14
DS1,2	
	Q2-18
	R2-4 6-37
S3,5	

05065-D-26

Figure 8-23. A14 Logic Assembly

POWER SUPPLY AND REGULATOR CIRCUIT A15 THEORY

The A15 Power Supply and Regulator Assembly provides regulated +20 V.

In addition, there are three other power supply circuits in the A15 Assembly:

a. The full-wave bridge rectifier, energized by chassis-mounted T1, which delivers +24 to 32 volts to the LC filter consisting of chassis-mounted L1, C1, and C2.

b. The magnetic field regulator which supplies dc current for the magnetic field winding in A12 RVFR Assembly according to the setting of the MAGNETIC FIELD control on the front panel.

c. The -20 volt supply.

In the +20 volt regulator, +24 to 32 volts connects to chassis-mounted Q1 and through A14(4) to the +20 volt regulator circuit. Regulated +20 volts connects to the voltage adjustment R17 which controls Q5A bias. The other side of differential amplifier Q5A and B is stabilized by Zener diode CR5 to provide a 9 volt reference. Q5 output is amplified by FET Q4, used as a source follower, and A15Q1 to provide bias control of chassis-mounted transistor Q1. In this way, Q1 output is held at +20 volts. Overcurrent protection is provided by the voltage drop of R2 which biases Q3 to drive Q2 and Q1; this turns off Q1. Ripple in the output at A15(8) is minimized by L2 and C11.

Full-wave bridge rectifier CR1 through CR4 is part of a basic power supply which includes chassis-mounted input transformer T1, and LC filter C1, C2, L1 and C7. The 24 to 32 volt output connects through a blocking diode on A18 circuit board to the 24 and 32 volt input of the +20 volt regulator circuit.

The magnetic field regulator consists of differential amplifier Q6A and B and Q7 which drives the magnetic field winding in A12 RVFR Assembly. This circuit works with the front-panel MAGNETIC FIELD dial to produce linear control of the resonant frequency of A12 RVFR Assembly. Since the resonance frequency is not directly proportional to magnetic field control, fixed resistances R8 and R12 pad the MAGNETIC FIELD potentiometer (R6) to provide the required linearity. Series reference resistors R10 and R11 provide Q6B with voltage information proportional to magnetic field winding current. Q6 differential amplifier drives Q7 to equalize Q6A, B base voltages. In this way, Q7 collector current through the magnetic field winding is a direct function of the voltage impressed on Q6A base by the front-panel MAGNETIC FIELD control.

In the -20 volt supply, +20 volts energizes the saturable transformer inverter circuit of Q8, Q9, and T1. The approximate 2 kHz output of T1 is full-wave rectified by CR6 and 7. C9 provides filtering. -20 volts connects to the output at A15(11) through voltage regulator Q10, whose base is referenced at about -20 volts by CR9A and B, and CR8.

A15 MAINTENANCE

NORMAL OPERATION

The A15 Assembly supplies the following voltages and currents to power the 5065A.

Pin No.	Voltage	Current
6	+20 V ± .2	700 mA
8	+20 V	130 mA
11	-20 V ± .2	25 mA
1,9 Adjustable	+2 to 4½	2.5 to 6 mA

In addition, the A15 Assembly has over-current protection circuit in the +20 V line.

OPERATIONAL CHECK

a. Using a dc voltmeter, check voltages at pins 6, 8, and 11. They should be as shown in the above table.

b. Connect voltmeter to pin 1 and (see NOTE) adjust MAGNETIC FIELD dial from 9 to 100. Voltage should be approximately as shown in the table.

NOTE
Be sure to note setting of MAGNETIC FIELD dial before making this adjustment. The dial should be returned to that setting after this test.

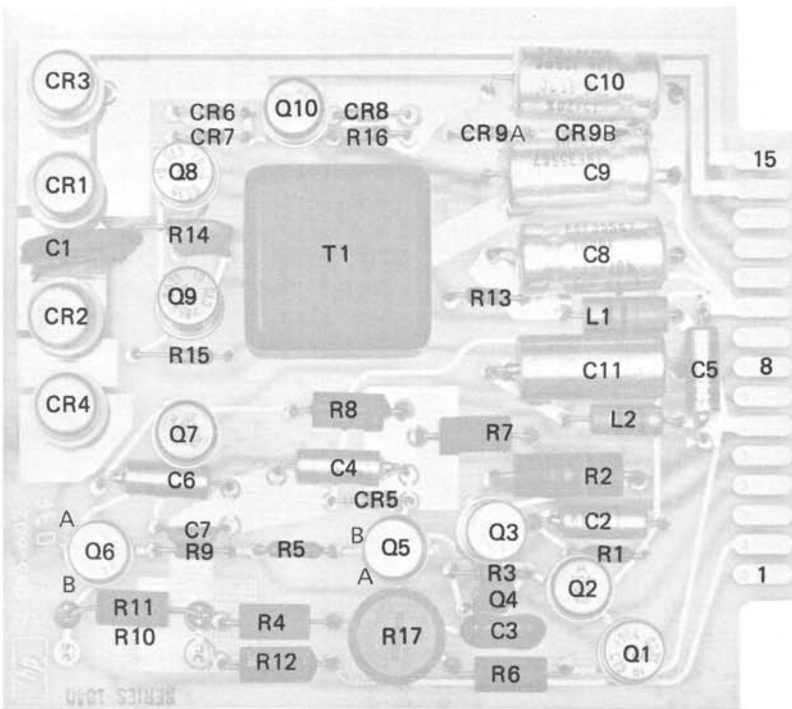
REPAIR AND ASSEMBLY REPLACEMENT

After making repairs, A15R17 should be adjusted. To do this place the A15 Assembly on the extender board provided and adjust R17 so that the voltage at A15(6) is 20 V ± .2 V.

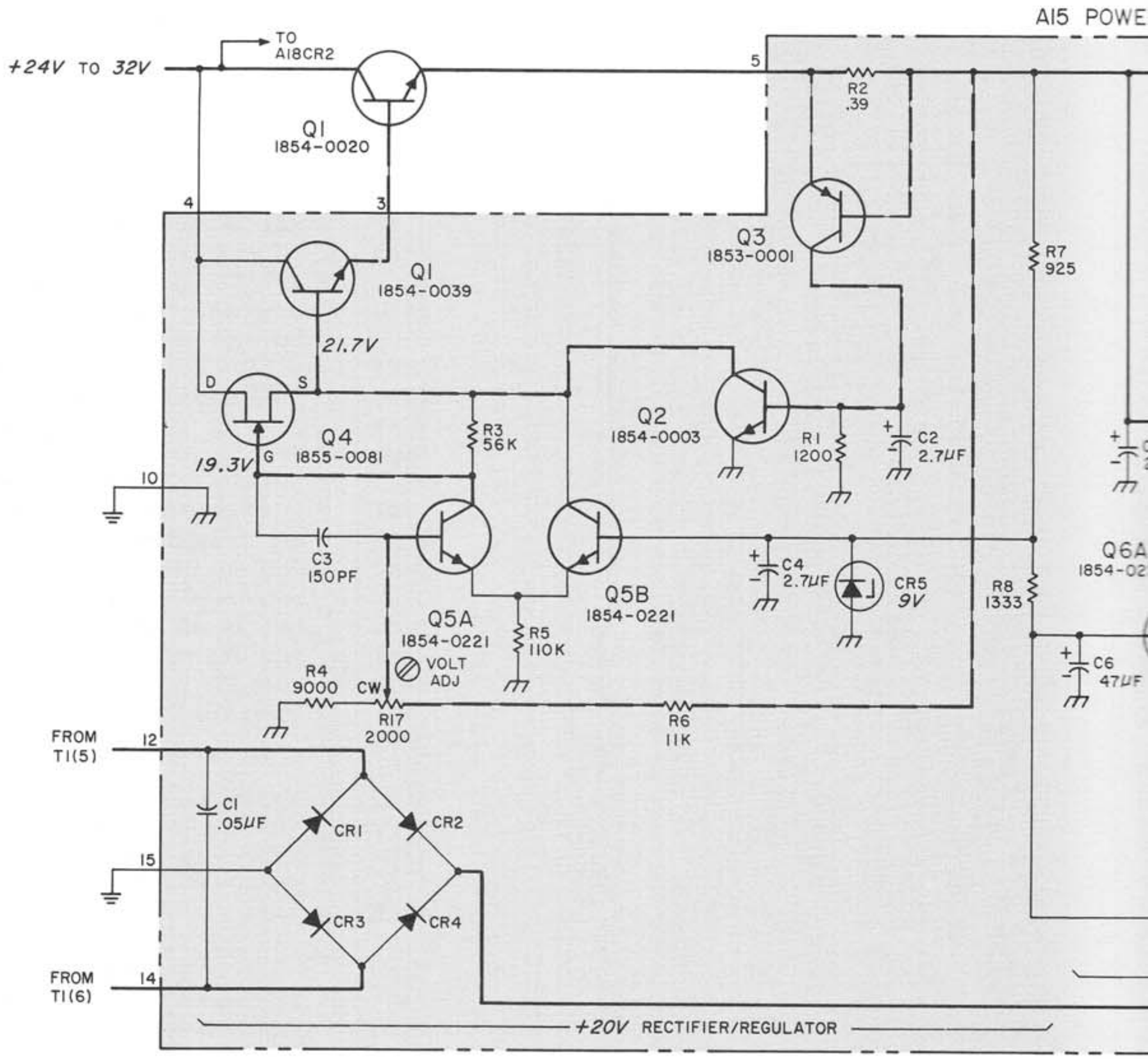
When replacing A15 the output voltage should be adjusted as described above. In addition, A15R10 and R11 should be removed from the old board and installed on the new one. This will help maintain the same magnetic field calibration.

Figure 8-24
A15 POWER SUPPLY AND REGULATOR ASSEMBLY

(See Page 8-65)



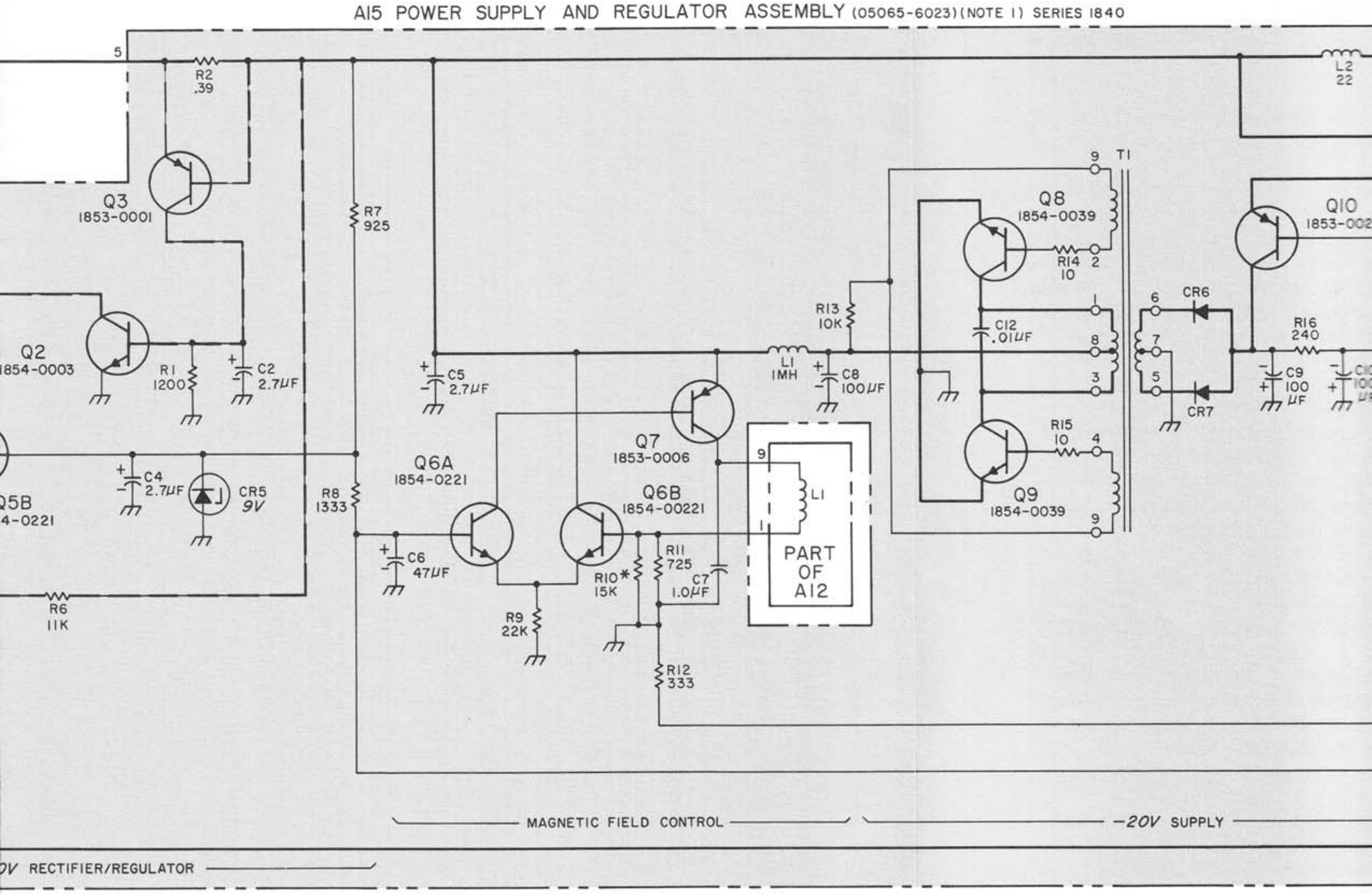
CR3
CR6
CR7
Q10
CR8
R16
C10
CR9A
CR9B
15
Q8
CR1
C9
T1
C1
R14
C8
Q9
R13
CR2
L1
R15
C11
C5
8
CR4
R8
Q7
R7
L2
C4
C6
R2
CR5
A
C7
C2
Q6
R9
R5
B
Q5
Q3
R1
1
B
A
R3
Q2
Q4
R11
R10
R4
R17
C3
Q1
R12
R6
SERIES 1010



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

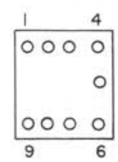
A15 POWER SUPPLY AND REGULATOR ASSEMBLY (05065-6023)(NOTE 1) SERIES 1840



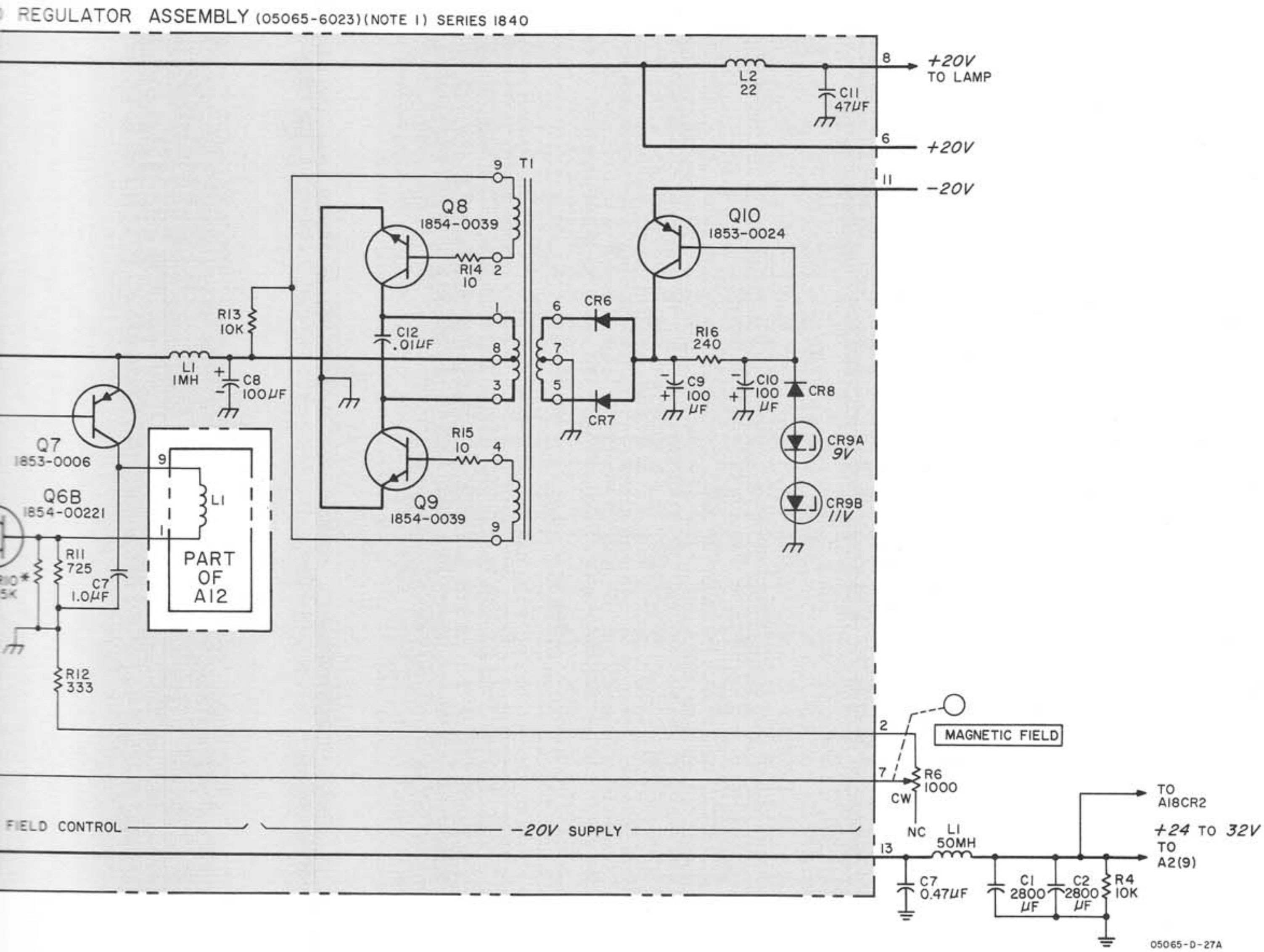
REFERENCE DESIGNATIONS

NO PREFIX	A12	A15
C1,2,7 CR3 J17 L1 P17 Q1 R4,6	 L1 T.E.D.	C1-12 CR1-9 L1,2 Q1-10 R1-17 T1

T1 OUTLINE



Figure



ERENCE DESIGNATIONS

	AI2	AI5
		CI-I2 CRI-9
	LI	LI,2
		QI-I0 RI-I7 TI
	T.E.D.	

TI OUTLINE

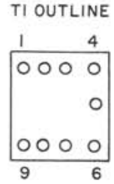


Figure 8-24. A15 Power Supply and Regulator Assembly

DIGITAL DIVIDER POWER SUPPLY A16 THEORY

The A16 module has three basic circuits:

a. Inverter and regulated power supply that supplies a +4.2 V output, and a +13.3 V zener-stabilized and filtered output for use in A16 circuits.

b. Blocking oscillator and output amplifier that supplies the 1 PPS tick pulse to the 1 PPS output jack.

c. The clock movement amplifier that supplies a push-pull square wave output to energize the clock.

The saturable-transformer, inverter oscillator of Q1, Q2, and T1 is powered by +20 V that is filtered by L1 and C1. R1, C2, and CR1 are a start circuit. R2, R3, C4, and C5 provide fast response, but limit average base current to improve inverter efficiency. Inverter frequency is about 1 kHz. Inverter output to the +4.2 V regulator is +6.5 V, full-wave rectified by CR2 and CR3, and filtered by C6.

In the regulator circuit, differential amplifier Q4 and Q6 compares a reference voltage developed by voltage divider R5 and R6 with the feedback dc voltage at the movable tap of +4.2 V control R13. Thus, the differential amplifier derives an error voltage. This error output at Q4 collector controls Q5 through Q3 to hold the regulated output at +4.2 V. Bypass elements R7 and C10 at Q5 base prevent oscillations. Further filtering for large load surges is provided by C17 and C18, with C17 providing high frequency filtering.

The second output of T1 energizes full-wave bridge rectifier CR4, 5, 6, and 7 to supply a positive dc output which is filtered by C7 and zener-stabilized at +13.3 V by CR8. Several elements of RC and LC filtering provided circuit decoupling.

Input 1 PPS pulses to the output tick blocking oscillator couple through J2 from A5 Digital Clock. Diode CR15 at Q7 base blocks any negative component of the input pulse. Q7 drives blocking oscillator transformer T2 and feedback to Q8 provides the regenerative action.

Diode CR9 protects Q7 and Q8 collector junctions. In T1 output, CR1 provides isolation. Selectable resistor R15 determines the output pulse width. Output tick pulses are provided by emitter followers Q9 and Q10. Zener diodes CR11 and CR12 limit output pulses to 10 volts peak. Q10 output is not used. Q9 output feeds the 1 PPS output jack.

1 PPS drive pulses connect from A5 Digital Divider through J1 to IC1 of the clock movement amplifier. IC1 provides flip-flop action and furnishes a push-pull output to clock amplifiers Q11 and Q12. The push-pull output of power amplifiers Q11 and A12 connects to the front panel clock and is limited to 10 V peak by zener diodes CR13 and CR14.

A16 MAINTENANCE

NORMAL OPERATION

The one-shot multivibrator output from A5A4, provides triggering for the Blocking Oscillator. This output is amplified and appears at J3 and a 1 PPS, 20 μs, +10 V pulse.

The power inverter provides +4.2 Vdc and +13.3 Vdc for A5 integrated circuits. Transistors Q1 and Q2 produce a 2 kHz pulse through T1 to the power supplies.

The output of A3Q15 is applied to clock movement flip-flop IC1. This flip-flop drives amplifier Q11 and Q12 which drives the clock movement.

OPERATIONAL CHECK

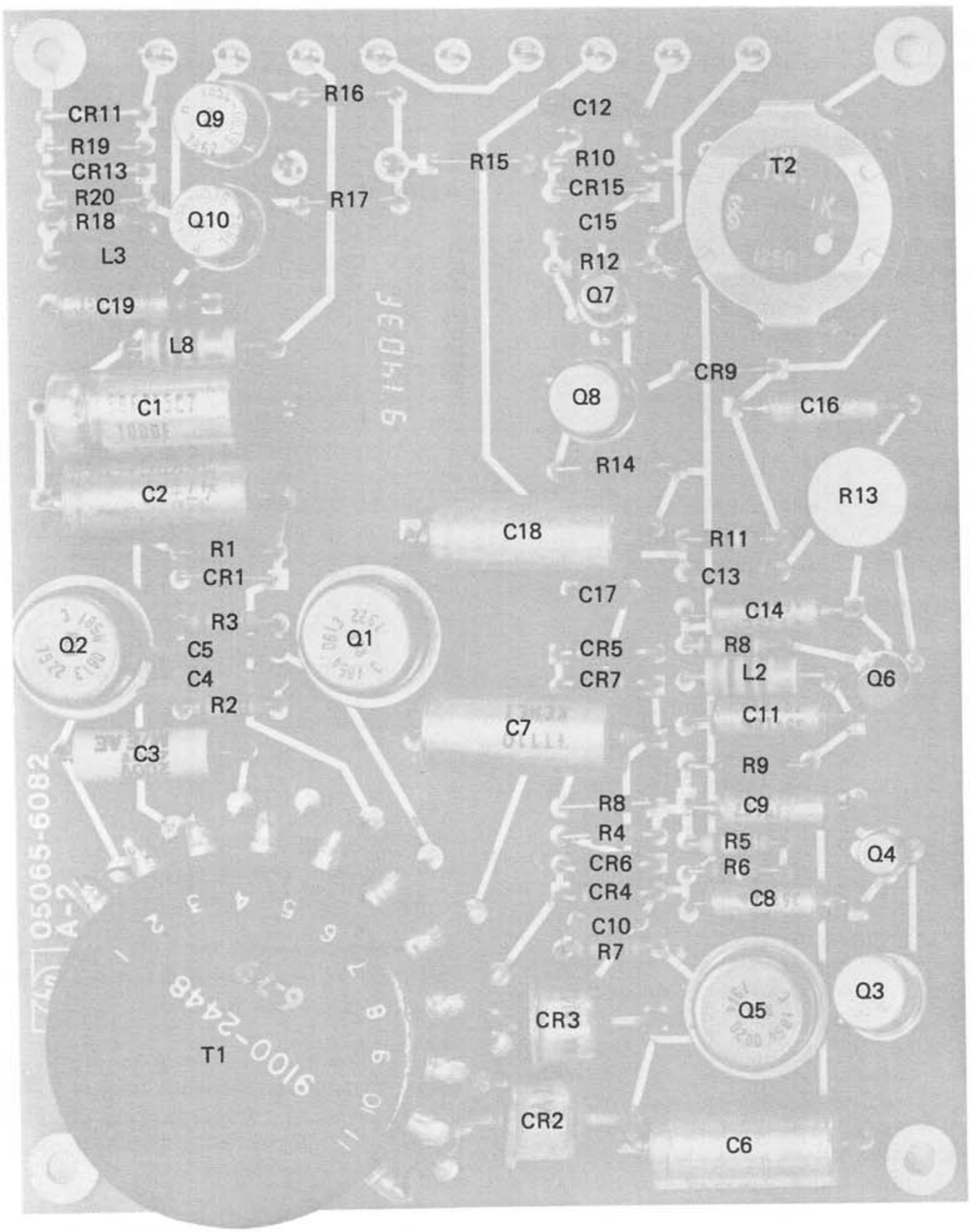
With unit power on, check with a dc voltmeter, for +4.2 V $\pm$.1 V across C17. Check for a +10 V, 20 μsec pulse at A16J3.

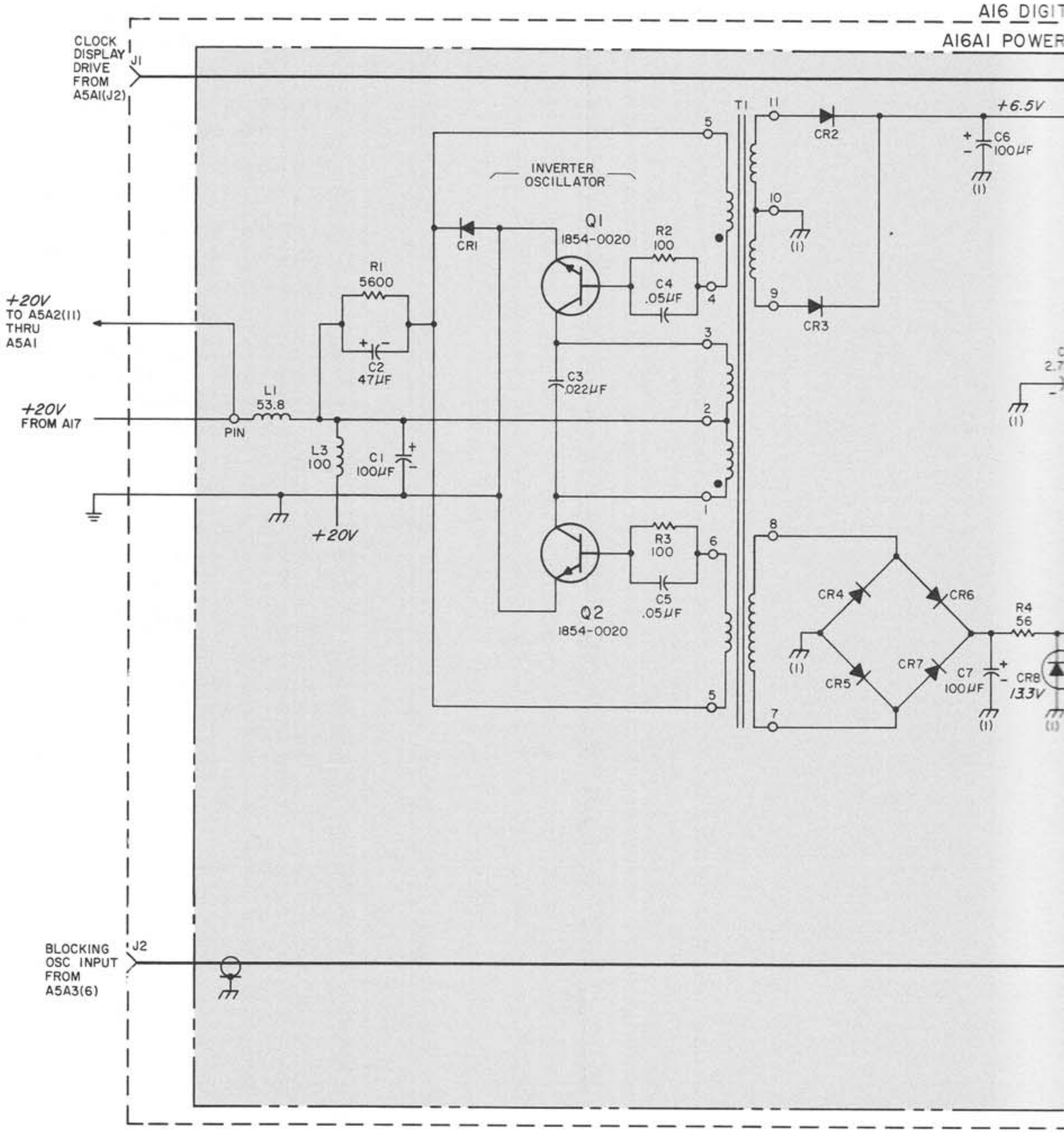
TROUBLESHOOTING

Digital divider power supply common is isolated from instrument common. To observe waveforms and measure divider voltages, divider common may be connected to instrument common for troubleshooting with no adverse effects.

Figure 8-25
A16 DIGITAL DIVIDER POWER SUPPLY ASSEMBLY

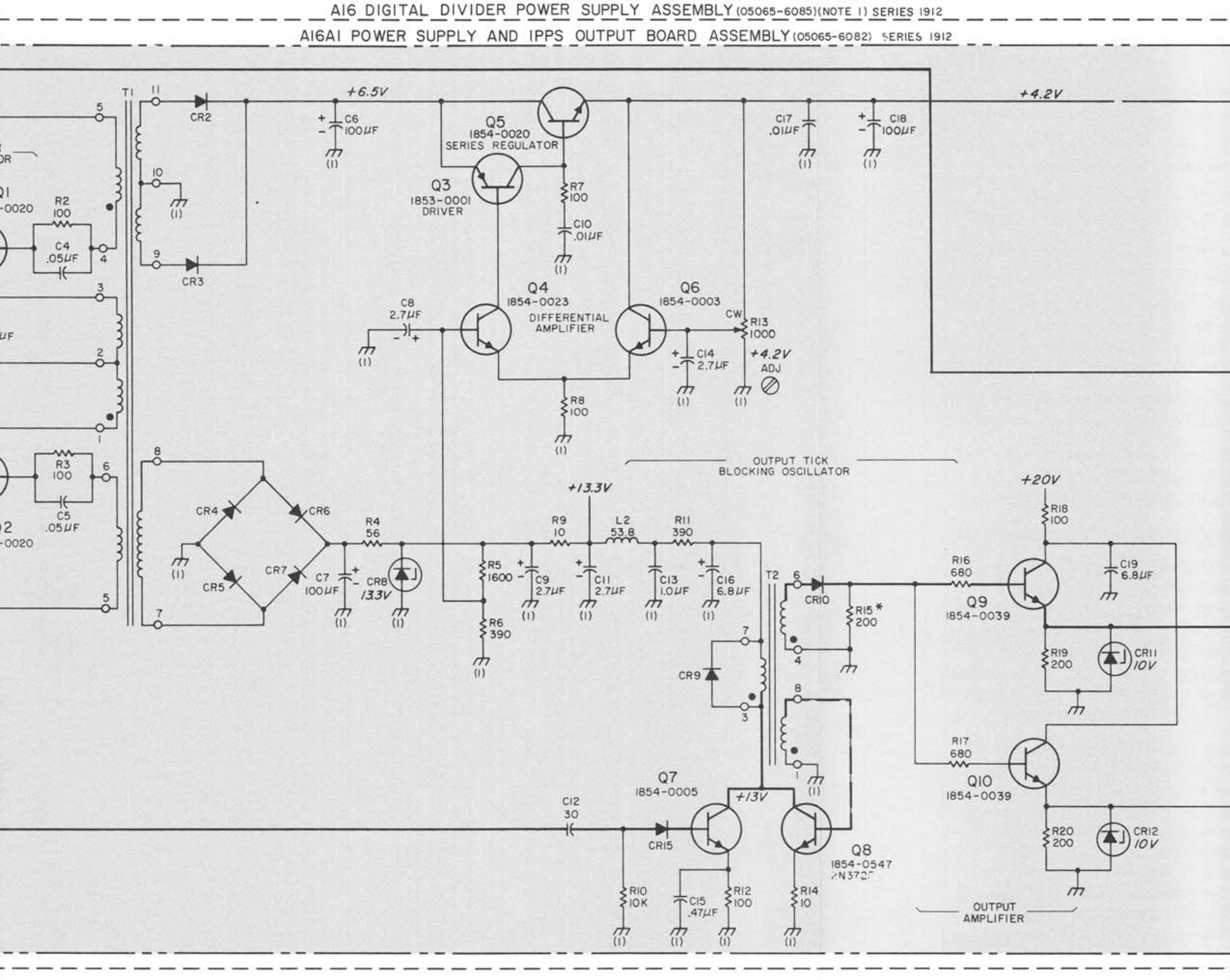
(See Page 8-67)


CR11
Q9
R16
C12
R19
R15
R10
T2
CR13
CR15
R20
Q10
R17
R18
C15
L3
R12
Q7
C19
L8
CR9
C1
Q8
C16
R14
C2
R13
C18
R11
R1
CR1
C13
C17
C14
R3
Q2
Q1
C5
CR5
R8
L2
Q6
C4
CR7
R2
C11
C7
C3
R9
R8
C9
R4
R5
CR6
R6
Q4
CR4
C8
C10
R7
Q5
Q3
CR3
T1
CR2
C6
05065-6082
A-2
9100-2448



NOTES

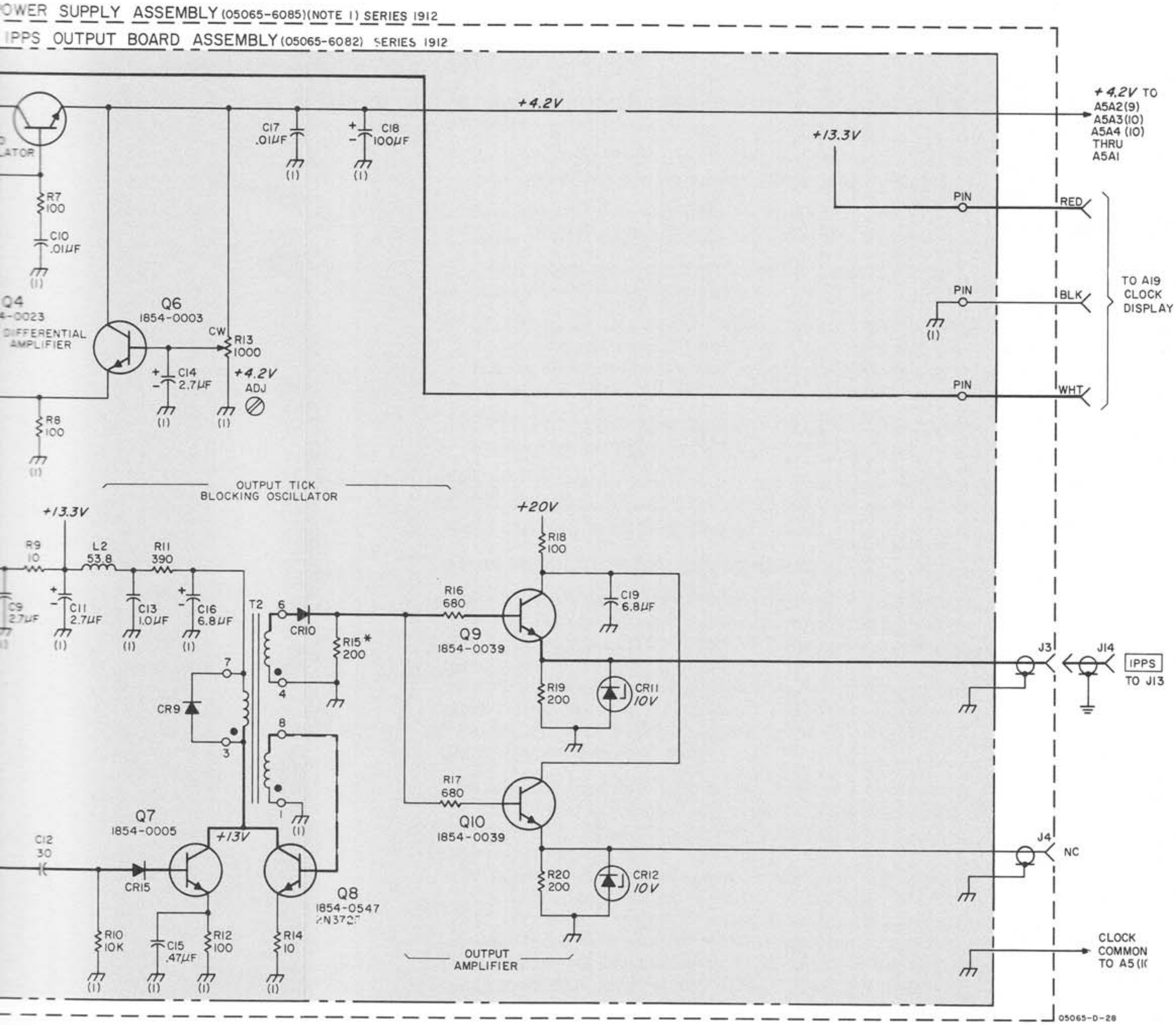
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK(*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN



REFERENCE DESIGNATIONS

NO PREFIX	A16	A16A1
J14	J1-4	C1-19 CR1-15 IC1 L1-3 Q1-12 R1-26 T1,2

Figure 8



REFERENCE DESIGNATIONS

	A16	A16A1
	J1-4	C1-19 CR1-15 IC1 L1-3 Q1-12 R1-26 T1,2

Figure 8-25. A16 Digital Divider Power Supply Assembly

CLOCK DISPLAY ASSEMBLY A19

The digital clock is a solid-state 24 hour clock with a seven segment LED (light emitting diode) display. It indicates time in hours, minutes, and seconds in synchronism with the 5065A generated 1 PPS signal. Time may be set and synchronized using the HOLD, SLOW/FAST, and SET switches.

The required inputs which enable the clock to operate are connected to the clock by five wires. These are:

1. Unregulated +28Vdc from the 5065A used to generate a regulated +5Vdc and used exclusively to drive the display.
2. Regulated +12Vdc from the A5 assembly used exclusively to operate the CMOS circuits in the display.
3. 1 PPS signal from the 5061A used to synchronize the clock and increment the display.
4. AC line sense signal from A2(9) turns off the display portion if instrument AC power fails or is removed. To display time, when AC power is not available, the clock front-panel STANDBY READ must be pressed.
5. 1 PPS and 12Vdc common. Circuit ground connects to the chassis through the LED digital clock circuits.

Two circuit boards make up the A19 Clock Display: the A19A1, Regulator/Driver (located at the rear of the A19 Assembly), and the A19A2, Display board.

A19A1 REGULATOR/DRIVER, GENERAL

The A19A1 Assembly contains two separate circuits. The regulator portion takes the unregulated 28Vdc from the 5065A and regulates it down to +5Vdc to provide power for the display light-emitting diodes. The driver portion takes the 1 PPS signal from the 5065A and shapes it for use by the clock accumulator/driver ship on A19A2. These two separate circuits are described in the following paragraphs under appropriate headings.

The regulator portion of the A19A1 Assembly consists of U2, Q3, Q4 and associated components. U2 is a switching regulator circuit that contains the switching oscillator, voltage reference, and switching transistor drive circuitry. The +5V regulator output voltage is sampled through R13 at U2(1). This voltage is compared to the reference input at U2(2). U1 adjusts the amount of time Q3 conducts based on whether the output voltage (+5V) is too high or too low. C9, L1, and C10 form a filter to keep switching transients out of the 5065A power supply. R9 and C7 set the switching frequency of the regulator. U2 provides a regulated +5Vdc at pin 16. This voltage provides the reference as well as providing power for Q2. L2 keeps current flowing to the load when Q3 is off. C14 and C15 filter the +5Vdc output. The circuitry of Q2 turns off the power supply to conserve power when the 5065A is operating from battery power. Under normal operation, when ac power is applied, zener diode CR1 conducts turning on Q2. This allows U2 to operate normally. When ac power is lost, Q2 turns off, forward biasing CR2 which in turn prevents the power supply from operating.

Pressing the STANDBY READ switch enables power supply operation, lighting the display. Current limiting and overvoltage protection is provided by Q4 and CR3, respectively.

The Clock Driver portion of the A19A1 Assembly operate in the following manner. A short (150 nsec) low level puls (≈1V) is applied to the input of Q1 from A16A1 (WHT This pulse is amplified (by Q1) and shaped by 555 timer U The output of U1 goes to A17A2 where it drives the cloc accumulator/display IC. In normal operation U1 behaves like a one-shot multivibrator outputting one pulse for each input pulse. When the SET pushbutton is activated, U1 free runs, and generates a signal whose frequency is set by th position of the SLOW/FAST switch. In SLOW, the frequency is approximately 60 Hz, 600 Hz in FAST. These two frequencies allow the hours, minutes, and seconds on th display to be easily set.

A19A2, CLOCK DISPLAY BOARD

The clock display board consists of a MOS cloc chip, a transistor array, a buffer amplifier array, four drive transistors, and six LED displays. This assembly's function is to accumulate and display time-of-day in synchronism with the instrument's 1 PPS signal. Operation is as follow The MOS circuit U1 normally operates from 50 or 60 Hz. It is enabled to operate by the 1 PPS signal from A19A1 by grounding the "slow set" line at U1 (17). U1 divides the PPS input to form the hours, minutes, and seconds cour In addition, it formats the output so that this count may be displayed on a seven-segment strobed LED display.

The time display signals from U1 are composed of tw parts:

1. The digit enable signal
2. The multiplexed seven-segment signal

The digits enable signals from U1 are:

Pin 23: tens-of-hours.
Pin 24: units-of-hours.
Pin 25: tens-of-minutes.
Pin 26: units-of-minutes.
Pin 21: tens-of-seconds.
Pin 22: units-of-seconds.

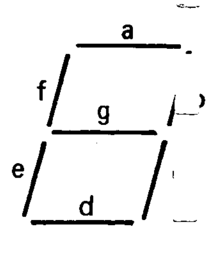
These signals enable the LED displays through U3 gate and allow the multiplexed seven segment outputs to turn the correct display segment.

The "segment enabling signals" are buffered through stages and applied to the LED displays. Thus, the segmer of an individual number display are enabled by outputs from U1 (6 to 12) while the display itself is turned on by one of the U1 (21 to 26) outputs.

The multiplexed seven-segment signals from U1 are shown below.

Legend:

Pin 6: for segment a.
Pin 7: for segment b.
Pin 8: for segment c.
Pin 9: for segment d.
Pin 10: for segment 3.
Pin 11: for segment f.
Pin 12: for segment g.



Repairs

Before attempting repairs, perform the following procedures:

NOTE

Some of the circuits on the CLOCK DISPLAY assemblies are CMOS. Use high impedance test equipment when checking signals. Precautions should be taken when removing or replacing these circuits to prevent damage from static charges.

a. Momentarily set front panel DIVIDER MODE switch to START.

b. Check CIRCUIT CHECK meter in 1 MHz position for reading of approximately 40. If reading not present, troubleshoot A6 assembly.

c. Check front panel 1 PPS output. If not present, troubleshoot A5 assembly.

d. If the display is not lit, press STANDBY DISPLAY switch. If display lights and operates normally, the instrument is not operating from AC power. This condition is normal. If the display does not light when the STANDBY DISPLAY switch is pressed, perform troubleshooting procedures described below.

e. Read A19A2 Clock Display Theory of Operation.

A19 Assembly Removal

Prior to removing or reinstalling the Clock Display, turn off all operating power. Wire and cable length to the clock panel or clock rear board is sufficient to permit removal of the clock without disconnecting these wires or the cable. Place the clock on a pad or cloth to minimize scratch damage or shorting of circuit traces. Then, proceed as follows:

a. Turn off all operating power.

b. Remove the instrument top cover. In Option 003 disable the internal standby battery.

c. Use a 5/16" spin-type wrench and remove three 5/16" nuts which secure the clock to the instrument front panel. Retain the nuts for reinstallation.

d. Press at the bottom-rear then at the top-rear of the clock until it is loose.

e. Carefully remove the clock. Gently pull the connected wires and cable forward and set the clock on the work surface.

f. With clock assembly removed, connect a jumper, or clip lead between the clock chassis and the instrument chassis.

g. Before applying operating power ensure that the exposed LED Clock boards and wires are not in contact with any metal objects or surfaces. Apply operating power.

h. To reinstall the Clock Display, turn off all operating power. In Option 003, disable the internal standby battery.

i. Perform steps b to e in reverse order. (See Note.)

NOTE

While installing the clock into the instrument front panel, check that wires are not pinched by screws or metal work. Position the wires for a neat appearance after installation.

j. When clock is reinstalled, apply power and set time as described in paragraph 3-28 of the 5065A Operating and Service Manual.

Troubleshooting

General

Procedures in this section describe fault isolation to the circuit board level, disassembly of the clock, and troubleshooting information for each of the three circuits.

Clock System Troubleshooting

To perform the following tests, remove the clock from the instrument and connect as described in A16 ASSEMBLY REMOVAL.

A19A1 Power Supply Check

NOTE

All voltages measured with respect to instrument chassis.

a. Measure voltages indicated below. Be sure to clock chassis is grounded to instrument chassis.

VOLTAGE	LOCATION
+26 ±4Vdc	A19A1P1(3)
+12 ±2Vdc	A19A1(R)
+5 ±.5Vdc	A19A1P1(4)

b. If the +26 or +12 volt supplies are out of tolerance, troubleshoot the source of these voltages. If the +5V supply is out of tolerance. remove the A19A2 Assembly and measure the voltage again. If voltage now is correct, go to step b(2).

(1) If voltage remains out of tolerance, troubleshoot A19A1, 5V regulator assembly.

(2) If voltage is now correct it indicates a short or low impedance on 5V line or defective current-limit circuit; troubleshoot 5V line and circuits on A19A2 which use 5V. If these are OK, check current-limit circuit of A19A1.

NOTE

An external 5V can be used in place of A19A1 output.

c. Check for +1V, 150 nsec, 1 PPS signal at A19A1(W). Be sure Clock Display chassis is grounded to instrument chassis. If pulse not present, troubleshoot A5 Digital Divider Assembly.

d. Check for 12V, .3 ms, 1 PPS signal at A19A1P1(5). If incorrect or not present, check circuit of A19A1U1.

A19A2 Clock Display Check

a. If display is not lit go directly to "Display Not Lit" step b. If display is lit but not functioning correctly, proceed as follows:

1. Check for 1 PPS signal at A19A2U1(19). It should be as shown on schematic. If not, troubleshoot Driver Circuit of A19A1U2.

2. Check operation of digit and segment drivers U2, U3 and Q1 thru 6. If these check OK, replace U1. See Note 4 on Figure 8-26 for typical waveform.

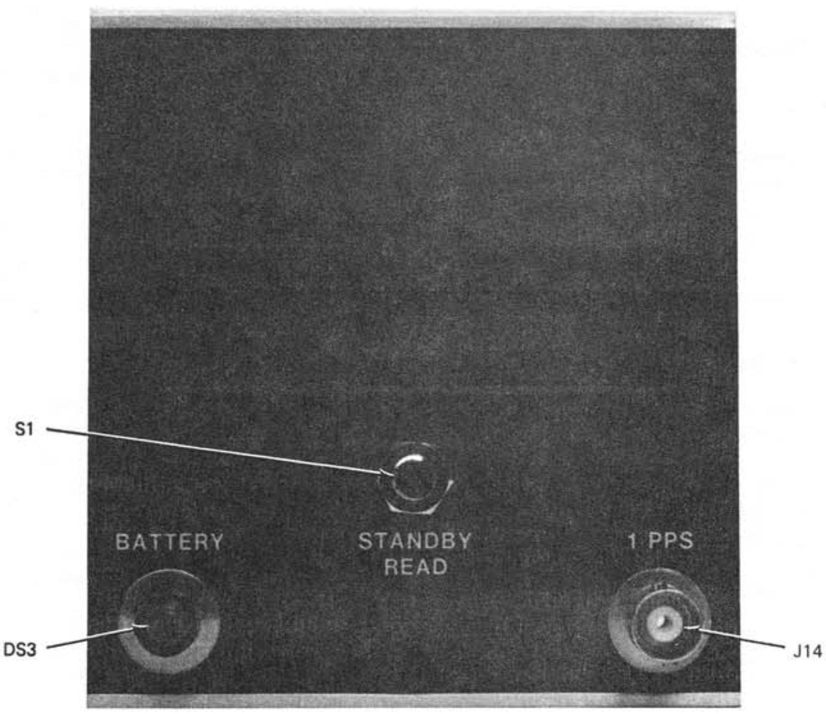
b. Display Not Lit

1. Check voltage at A19A2(4). It should be 5V ±.5Vdc. If incorrect, troubleshoot circuit of A19A2U1.

2. Check +12V input at A19A2(5). It should be the same as measured at "R" terminal on A19A1. If not, check continuity of +12V line from A19A1 to A19A2.

3. Substitute a new LED in one of the display positions.

4. Trouble is in A19A2U1 or 2. Check for switching waveforms at U1 (6-12) and (21-26). Check for switching waveforms at U2 and U3 outputs. See Figure 8-26 for typical waveforms.

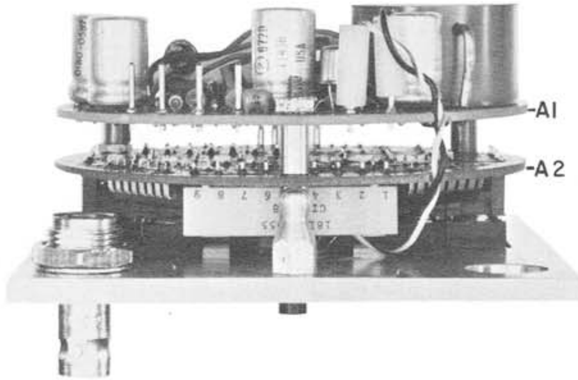


A19 FRONT PANEL

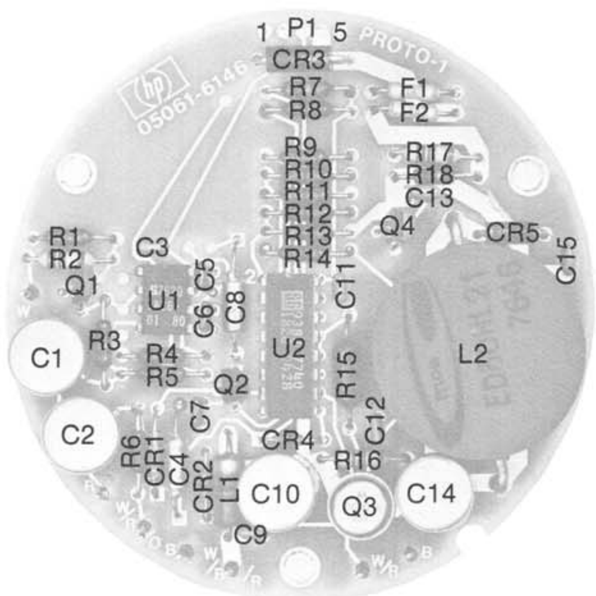
Figure 8-26
A19 CLOCK DISPLAY ASSEMBLY

(See Page 8-71)

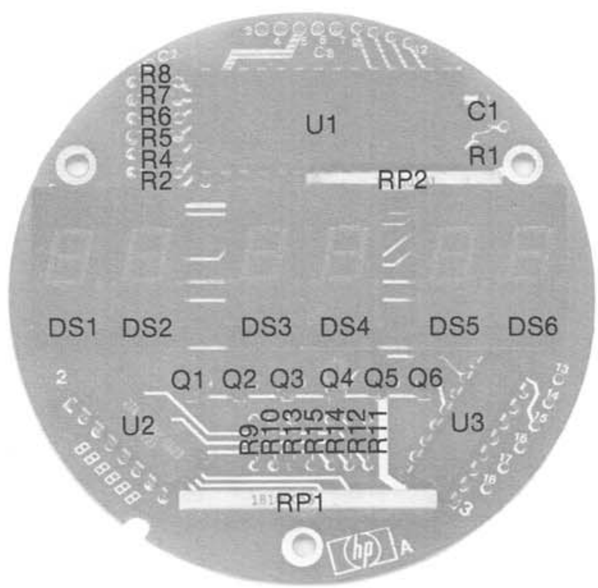
A19 CLOCK DISPLAY
SIDE VIEW

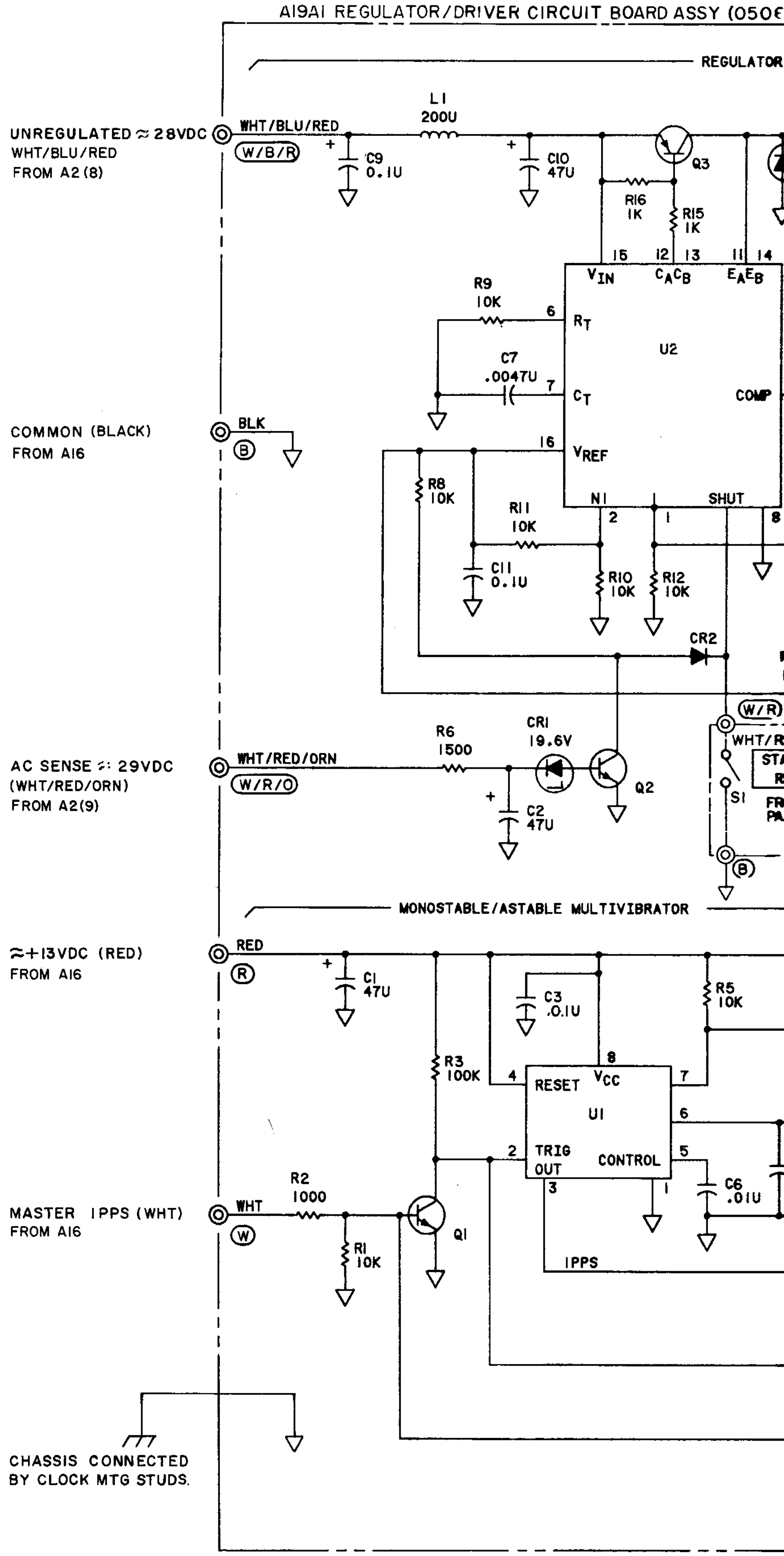


A19A1
REGULATOR
DRIVER

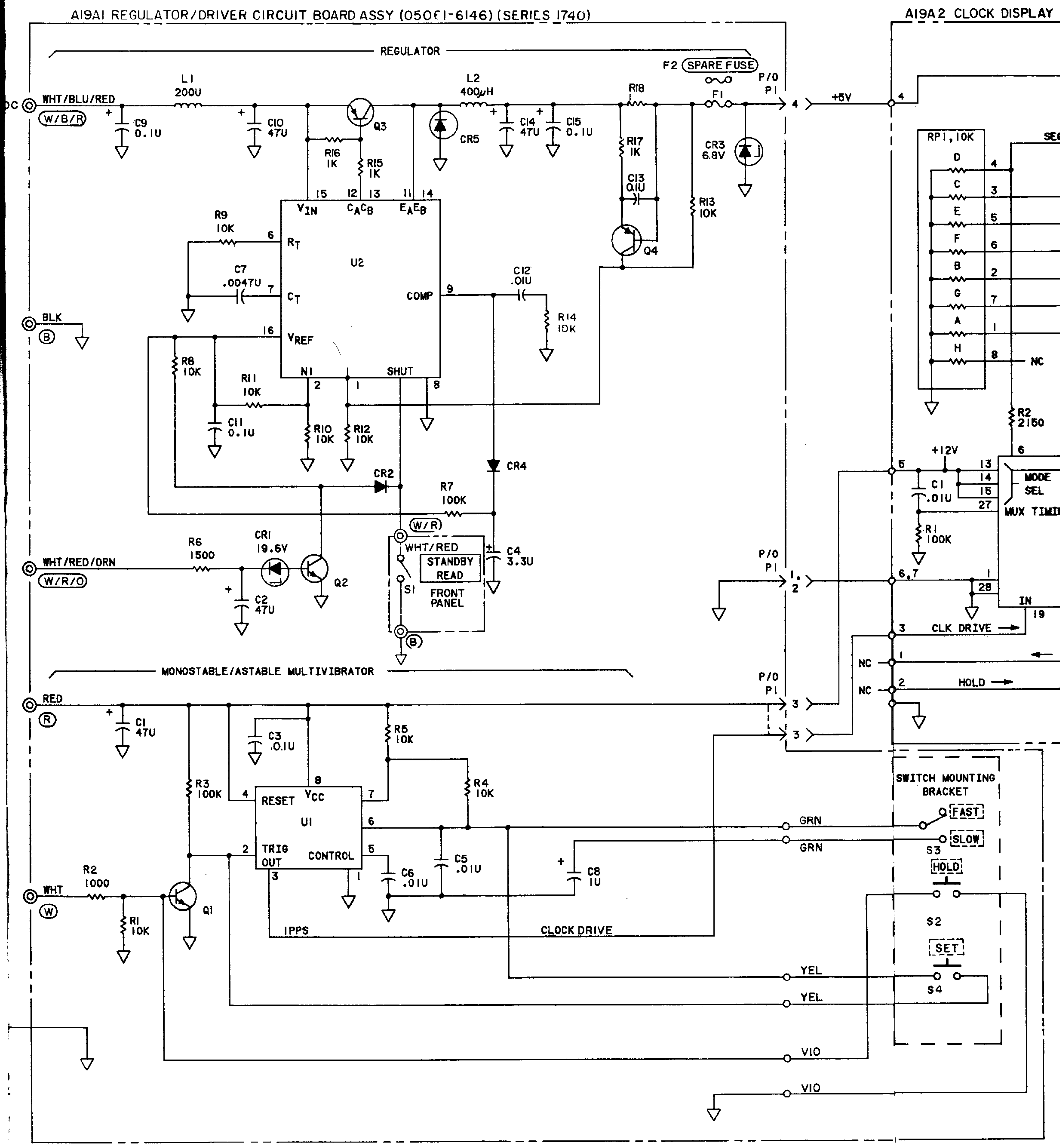


A19A2
CLOCK DISPLAY



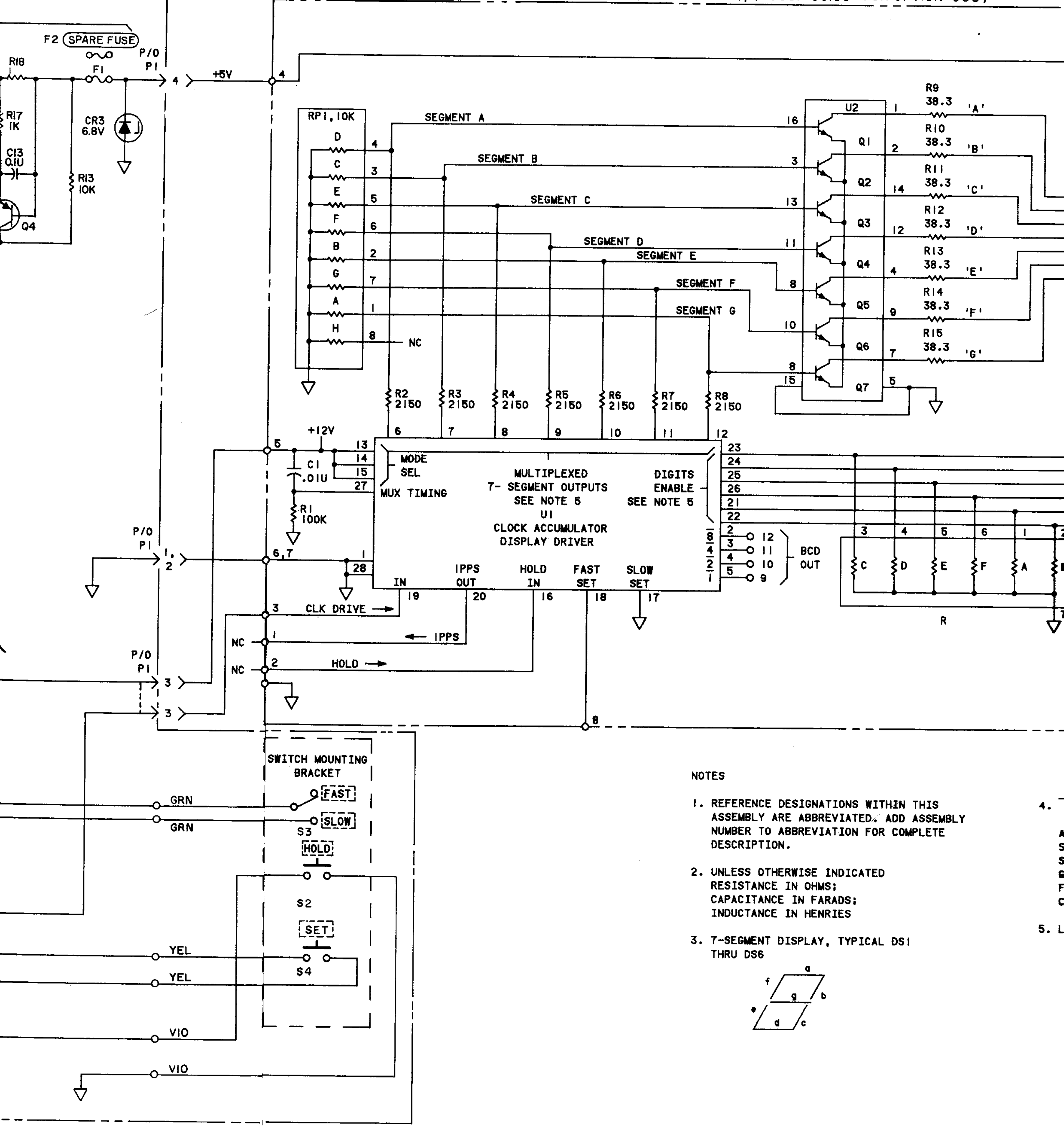


A19A1 REGULATOR/DRIVER CIRCUIT BOARD ASSY (050
REGULATOR
UNREGULATED ≈ 28VDC
WHT/BLU/RED
FROM A2(8)
WHT/BLU/RED
W/B/R
L1
200U
C9
0.1U
C10
47U
Q3
R16
1K
R15
1K
R9
10K
C7
.0047U
U2
COMP
COMMON (BLACK)
FROM A16
BLK
B
R8
10K
R11
10K
C11
0.1U
R10
10K
R12
10K
CR2
AC SENSE ≈ 29VDC
(WHT/RED/ORN)
FROM A2(9)
WHT/RED/ORN
W/R/O
R6
1500
CR1
19.6V
C2
47U
Q2
W/R
S1
MONOSTABLE/ASTABLE MULTIVIBRATOR
≈+13VDC (RED)
FROM A16
RED
R
C1
47U
C3
.0.1U
R5
10K
R3
100K
RESET
U1
TRIG
OUT
CONTROL
C6
.01U
MASTER 1PPS (WHT)
FROM A16
WHT
W
R2
1000
R1
10K
Q1
1PPS
CHASSIS CONNECTED
BY CLOCK MTG STUDS.



A19A1 REGULATOR/DRIVER CIRCUIT BOARD ASSY (05061-6146) (SERIES 1740)
A19A2 CLOCK DISPLAY
REGULATOR
WHT/BLU/RED
W/B/R
L1 200U
C9 0.1U
C10 47U
R16 1K
R15 1K
Q3
L2 400μH
CR5
C14 47U
C15 0.1U
R18
F2 SPARE FUSE
F1
P/O P1
+5V
R17 1K
C13 0.1U
CR3 6.8V
R13 10K
Q4
R9 10K
C7 .0047U
U2
VIN
CACB
EAEB
RT
CT
COMP
VREF
NI
SHUT
C12 .01U
R14 10K
BLK
B
R8 10K
R11 10K
C11 0.1U
R10 10K
R12 10K
CR2
CR4
R7 100K
W/R
WHT/RED
STANDBY
READ
S1
FRONT PANEL
C4 3.3U
WHT/RED/ORN
W/R/O
R6 1500
CR1 19.6V
Q2
C2 47U
RP1, 10K
R2 2150
NC
+12V
MODE SEL
MUX TIMI
C1 .01U
R1 100K
IN
CLK DRIVE
HOLD
MONOSTABLE/ASTABLE MULTIVIBRATOR
RED
R
C1 47U
C3 .0.1U
R5 10K
R4 10K
R3 100K
RESET
VCC
U1
TRIG
OUT
CONTROL
C6 .01U
C5 .01U
C8 1U
WHT
W
R2 1000
R1 10K
Q1
1PPS
CLOCK DRIVE
GRN
YEL
VIO
SWITCH MOUNTING BRACKET
FAST
SLOW
S3
S2
SET
S4

A19A2 CLOCK DISPLAY ASSEMBLY (05061-60125 FOR OPTION 001), (05061-60136 FOR OPTION 003)



NOTES

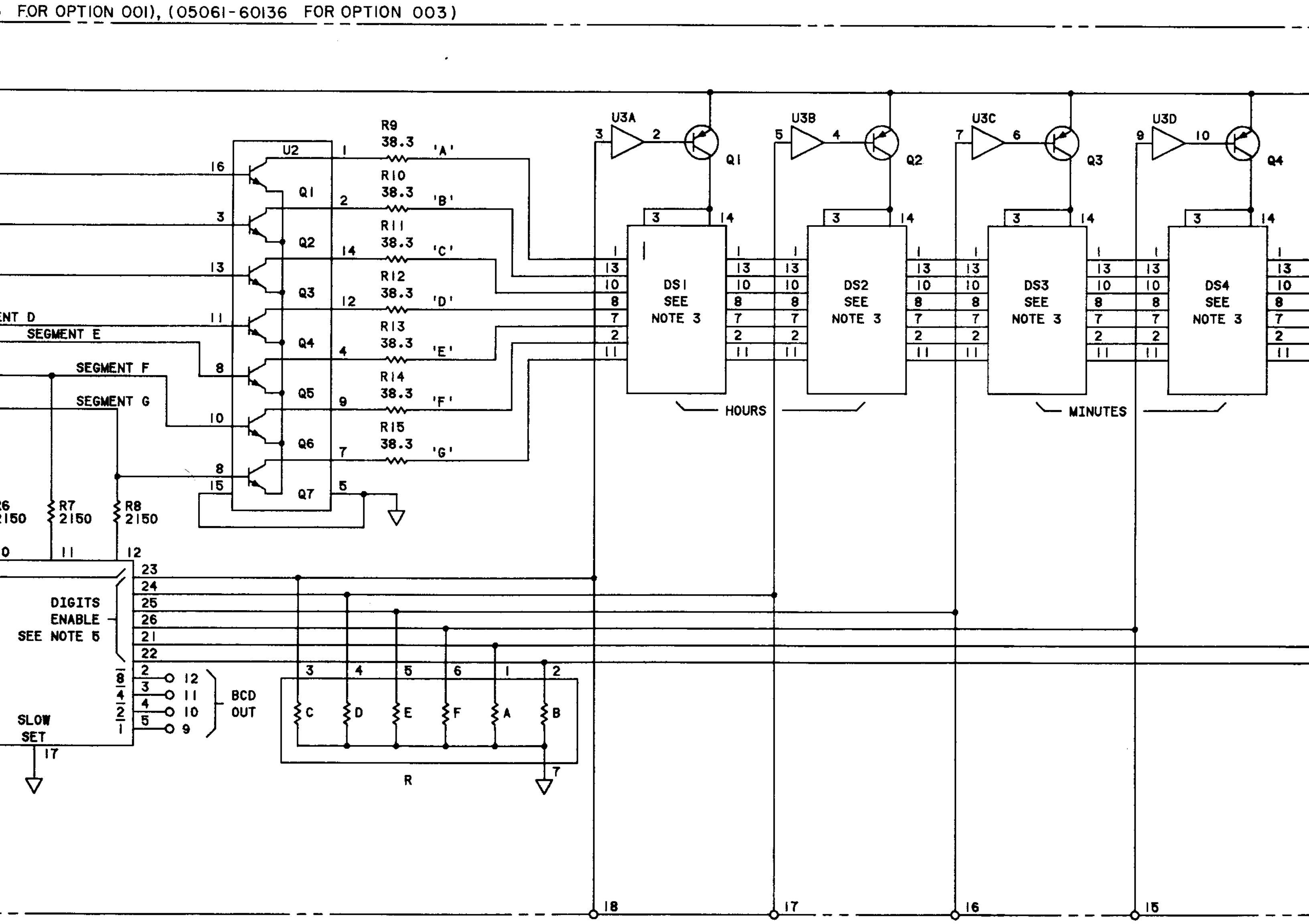
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES

3. 7-SEGMENT DISPLAY, TYPICAL DS1 THRU DS6

4.

5. L

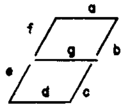


NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED RESISTANCE IN OHMS; CAPACITANCE IN FARADS; INDUCTANCE IN HENRIES

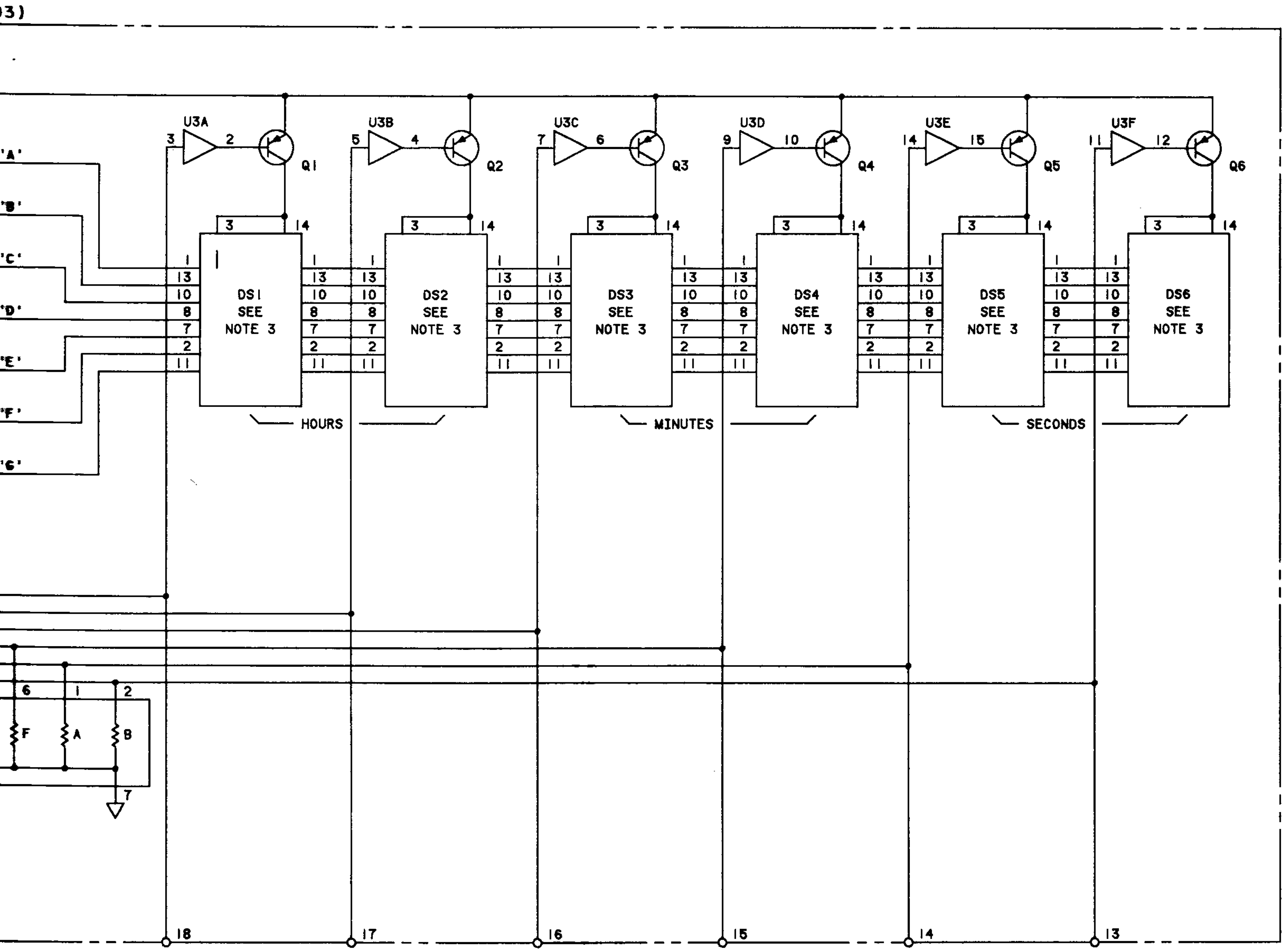
3. 7-SEGMENT DISPLAY, TYPICAL DS1 THRU DS6



4. 

APPROXIMATION OF DISPLAY AND SEGMENT SWITCHING WAVE FORM IN SOME CASES THE SAME SEGMENT IS OFF IN ALL DISPLAY GIVING A STRAIGHT LINE WAVE FORM. WAVE-FORMS WILL CHANGE EACH SECOND WITH CLOCK RUNNING.

5. LEGEND: ◎ POST TERMINALS
O WIRE SOLDERED IN BOARD



4. 

APPROXIMATION OF DISPLAY AND SEGMENT SWITCHING WAVE FORM IN SOME CASES THE SAME SEGMENT IS OFF IN ALL DISPLAY GIVING A STRAIGHT LINE WAVE FORM. WAVE-FORMS WILL CHANGE EACH SECOND WITH CLOCK RUNNING.

5. LEGEND: ◎ POST TERMINALS
O WIRE SOLDERED IN BOARD

Figure 8-26. A19 Clock Display Assembly

HEWLETT PACKARD

MANUAL PART NO. 05065-9041

PRINTED IN U.S.A.

DIGITAL DIVIDER A5 THEORY

GENERAL DESCRIPTION

The A5 Digital Divider provides a one pulse-per-second signal for a front and rear panel output signal, and drives the A19 Clock Display Assembly. The 1 PPS output can by synchronized to an external 1 PPS signal with selectable time delay difference with respect to an external synchronizing 1 PPS.

A5 has four subassemblies:

1. A5A1 Multiplier and Amplifier
2. A5A2 Voltage Regulator
3. A5A3 10 MHz-to-1 PPS Divider And Delay
4. A5A4 Interconnect

The four subassemblies are described in the following paragraphs.

A5A1 Multiplier-Amplifier

The A5A1 Multiplier and Amplifier has three separate parts: 1) a 1 MHz-to-10 MHz multiplier, 2) an amplifier, and 3) a drive for the A19 Clock Display.

The multiplier section provides a 10 MHz output signal generated from the 1 MHz input signal supplied by A6. The 1 MHz signal, which comes in on the J4 RF connector, is coupled through C1 to the base of Q1. Q1, which is part of the differential amplifier Q1-Q2, acts as a switch. The input signal is switched through L2 to generate 1 MHz harmonics. CR1 prevents ringing in the signal that could damage Q2 and Q3. The output of Q2 is connected to Q3, which is a tuned amplifier at the resonant frequency of L1 and C4. The output of Q3 is applied to another amplifier (Q4-Q5) tuned to 10 MHz by L3. At this point, a good 10 MHz sine wave has been generated. The output of Q5 is coupled through C10 to the input of the sine wave-to-TTL converter, Q6-Q7. When the signal is above the dc bias of Q6, Q6 switches off, switching Q7 on. This generates a TTL-high pulse at $\overline{A5A1(12)}$ that follows the 10 MHz sine wave from Q5. Diode CR2 produces the dc bias voltage for Q1, Q2, Q4, Q5, Q6, and Q7.

The amplifier section of A5A1 has an amplifier that converts the 1 PPS signal from A5A3 to TTL for the front-panel 1 PPS output connectors. Transistors Q8, Q9, and Q11 comprise this amplifier.

The third section of A5A1 has a single transistor amplifier, Q14, that drives the A19 Clock Display with the 1 PPS signal from A5A3. U1 is a regulator that transforms an input of +18 Volts to +12 Volt power for the A16 Clock Display Assembly.

The A5A1 assembly is a connection point for signals from the HP 5065A making them available for external use. Connector J4 has the 1 MHz input sine wave, at about 1 Volt rms, that is applied to a 10 MHz multiplier. The 10 MHz signal at $\overline{A5A1(12)}$ is connected through A5A4 to $\overline{A5A3(12)}$. The SYNC signal from J12 on the 5065A rear panel is connected through A5A1 to A5A4 and then to A5A3(1). The 1 PPS signal from A5A3 is synchronized with the SYNC signal from the 5065A rear panel. The other RF connector, J1, is a 1 PPS output. The 1 PPS from A5A1J1 is connected to J13 on the 5065A front panel. There are four terminals on A5A1. Terminal 4 is the +18 Volt input terminal and has a red wire connected to it. Terminals 1, 2, and 3 are outputs to the A19 Clock Display. Pin 1 is common (ground). Pin 2 is the +12 Volt power. Pin 3 is the 1 PPS signal that drives the front-panel clock display.

A5A2 5-Volt Regulator

The A5A2 assembly receives the +18 Volt power from A5A1 and regulates it to +5 Volts for A5A1 and A5A3. There are three basic circuits in A5A2:

1. voltage reference
2. switching regulator
3. short-circuit current protection

U3 is a voltage reference that supplies +2.5-Volt reference to the non-inverting input [U2(2)] of the switching regulator. Feedback from the regulator output to U2(1) through voltage divider R12-R13, drives U2(1) to the same voltage as U2(2); +2.5 Volts. So the output must be +5 Volts because R12 and R13 are almost equal.

The U2 regulator oscillates at about 25 kHz. This signal, which is set by R7 and C4, switches Q2-Q1 on and off. When Q1 is on, current is forced through L1 because CR1 is reverse-biased. When Q1 switches off, the polarity of L1 reverses to keep current from flowing from ground, through CR1 and L1, and to the load. The output voltage is regulated by U2 adjusting the time that Q1 is switched on for every cycle. In normal operation, the duty cycle is about 35 percent. A soft start is provided by C6, R11 and CR3. C5 and R10 provide compensation for the internal U2 operational amplifiers.

Short-circuit protection is provided by U1. During normal operation, the voltage at U1(2) is greater than the voltage at U1(3) (about +5.08 Volts and +4.95 Volts). Therefore the output of U1 is low. When the load current through R1 is greater than 950 milliamperes, the voltage at U1(2) is less than the voltage at U1(3). The output of U1 goes up to about +3 Volts and switches U2 off through R14. U1 will keep U2 switched off while the short-circuit condition continues.

A5A3 10 MHz-to-1 PPS Divider and Delay

The A5A3 board generates a one pulse-per-second signal that provides the front-panel 1 PPS output. The 1 PPS is synchronized to an external signal from the rear-panel

SYNC INPUT connector. The 10 MHz from A5A1 is applied to all of the decade counters, U8 through U14. ENABLE P and ENABLE T (Pins 7 and 10) of U11 are always enabled (always held high). Therefore, every time the clock pulse occurs, that counter changes state. The least significant bit in this counter chain is pin 14 of U11. If this point is monitored with an oscilloscope, a 5 MHz signal is displayed. U11 pin 13 has a 2 MHz signal, and pin 11 has a 1 MHz signal. Pin 15, the ripple-carry output of U11, also has 1 MHz. The U11(15) output is not a square wave. It is approximately a 100-nanosecond pulse that occurs every microsecond. During the one clock period that U11(15) is held high, pins U14(10 and 7) are enabled, and U14 is clocked one time. Then the ripple-carry output of U11 goes low again disabling U14. Later clock pulses do not change U14 until the ripple-carry output of U11 once again goes high ten cycles later. This occurs all the way up the chain to U8, which has the most significant bits, and U8(11) is actually pulsing at a 1 Hz rate. The signal from U8(11) is used to generate the non-delayed 1 PPS. This signal is not used in A5; it is used only for factory testing.

TIME DELAY Switches and Dividers Operation

The A5A3 Digital Divider has seven thumbwheel switches that allow the delay to be set in 100-second steps. When all thumbwheels are set to zero, the delay between the reference pulse and the delayed pulse is 100 nanoseconds plus or minus 100 nanoseconds. An example of how this circuit works is demonstrated by looking at switch S1 which is compared to the outputs of U11. If S1(10) is low and S1(11) high, pin 7 low, and pin 2 high, then when U11(14) goes high while S1(10) is low, these two outputs have different states and the output U7(3) goes high (U7 is an exclusive OR gate). In the same way, if all of the outputs of U8-U14 were opposite to what they are being compared to, then all outputs of the exclusive OR gates would go high simultaneously. That is, if U11(14) were in the complementary state of S1(11), and that condition was the same all the way through this set of exclusive OR gates (U1-U7), there would not be any open collector outputs that are pulled low and so a pulse would be sent to U18B. This happens once every second when the output state of U8-U14 is exactly the opposite in the absolute sense of the switch settings. This generates the delay that the operator desires.

A5A4 Interconnect

The A5A4 Interconnect Board provides electrical connections between the A5A1, A5A2, and A5A3 subassemblies of the A5 Digital Divider. There are no active circuits on A5A4.

A5 DIGITAL DIVIDER MAINTENANCE

The A5 Digital Divider provides one pulse-per-second output signals at the HP 5065A front panel, and to the front-panel digital clock. A 1 MHz signal from the A4 100 kHz Frequency Divider is the input signal to A5.

A5 Preparation for Troubleshooting and Adjustments

The A5 Digital Divider can be removed from the chassis for servicing. The extender board supplied with the HP 5065A (HP Part Number 05061-6073) can make circuit parts accessible for testing. Use the following procedure to remove A5 from the chassis for troubleshooting and adjustment:

NOTE

A5 can be removed from the chassis with the power still applied to the HP 5065A. Be careful of the high-voltage terminals inside the 5065A cabinet. Extender board (HP Part Number 05061-6073 in accessory kit) makes A5 components accessible.

a. Remove the cabinet top and bottom covers.

b. Disconnect the three coaxial connectors (J1, J2, and J3) from the A5 module at the bottom of the chassis. Disconnect the four single wires (B, R, W, and R) from the A5 module at the bottom of the chassis.

c. Remove the screws that hold the A5 module in the chassis, and carefully remove the A5 from the chassis.

d. Remove the screws that hold the A5 module shield cover, and remove the cover.

e. Reconnect cables and wires to supply power signal connections to A5.

f. Keep the A5 assembly in a position such that no electrical connections are short-circuited.

g. After repairs and adjustments are complete, replace the A5 Divider in its normal position in the 5065A chassis.

A5 Adjustments (Tuning)

Use the following procedure to check and adjust the A5 Divider after repair or replacement with a new unit:

a. With the A5 Divider out of the chassis and set up for maintenance, connect the vertical input of an oscilloscope to the junction of A5A1L1 and A5A1Q3. The oscilloscope display should be a 10-MHz sine wave signal with ten cycles that decay from about 3 to 4 Volts peak-to-peak to some small amplitude, and then the decaying waveform repeats continuously.

b. Adjust L1 with a nonmetallic tool for maximum signal on the oscilloscope.

c. Connect the oscilloscope to the junction of A5A1L3 and A5A1Q5. The oscilloscope display should be a 10-MHz sine wave signal at about 5 to 6 Volts peak-to-peak.

d. Adjust L3 with a nonmetallic tool for a maximum signal on the oscilloscope. Then adjust L1 again for maximum signal at L3-Q5 junction.

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 8-33, Figure 8-13. A5 Digital Divider Assembly (Option 001)(Sheet 1):

All Serials	>Change label at A5A1J1, left side of diagram to, "1MHz FROM FREQ DIV A4(2)". >Change label at A5A1J2 to "CLOCK DRIVE TO A16". >Change pin numbers 4 and 6 for A5A5XA3 and A5A4XA4; pin 6 should be "4" and pin 4 should be "6" on both sockets. REFERENCE DESIGNATIONS table: >Change S1-3 to S2, under A5. >Change C1,2 and R1-3 to C1 and R1-4 (respectively) under A5A4.
2144A	>Change A5 SERIES to 2144. >Change A5A3 from 05061-6013 to 05061-6167, SERIES 2144.
2208A	>Change A5 SERIES to 2208.

Page 8-35, Figure 8-14. A5A2 Master Clock Board (Option 001) (Sheet 2 of 3):

All Serials	>Change Reference Designator for resistor R48 to R42. >Change Reference Designator for resistor R42 to R43. >Change A5A2IC1, IC2, and IC3 part numbers to 1820-0580.
2144A	>Change A5A2 SERIES to 2144.
2208A	>Change A5A2 SERIES to 2208.
2308A	>Replace A5A2 schematic, component locator, and tables with new page 8-35 (SERIES 2308) supplied in this manual change.

Page 8-37, Figure 8-15. A5A3 Preset Clock Board (Option 001) (Sheet 3 of 3):

All Serials	>Change label at A5A3 pin 6 by deleting "OUTPUT, TICK, BLOCKING & OSCILLATOR". >Change "A5A1(3)" at label for A5A3 pin 7 to A5A1(8). >Change A5A3IC13, IC15, and IC16 part numbers to 1820-0580. >Change the value of A5A2 L1 and L3 to 51 microhenries.
2144A	>Replace A5A3 (05061-6013) schematic, component locator, and tables with new A5A3 (05061-6167, SERIES 2144) schematic, component locator and tables supplied in this manual change.
2208A	>Change A5A3 SERIES to 2208.
2308A	>Replace A5A3 schematic, component locator, and tables with new page 8-37 (SERIES 2308) supplied in this manual change.

SERIAL PREFIX OR SERIAL NUMBER	CHANGES

Page 8-41, Figure 8-16. A6 1 MHz Frequency Divider Assembly:

All Serials	Component Locator: >Change reference designation of capacitor in lower left corner from Q6 to C26.

Page 8-47, Figure 8-18. A8 Phase Detector Assembly:

All Serials	>Add ferrite beads E1, E2, and E3 at bases of Q8, Q9, and Q10 respectively.
2740A	>Change A8 (05065-6013) SERIES to 2740. (See A8 parts list for change.)
2816A	>Change A8 (05065-6013) SERIES to 2816. (See A8 parts list for change.)

Page 8-48. Circuit Diagrams, Theory, and Maintenance:

All Serials	>Replace all of Operational Amplifier A9 Theory with the Operational Amplifier A9 Theory in these manual changes. A9 MAINTENANCE: >Replace all of NORMAL OPERATION; replace paragraphs c., e., and g. of OPERATIONAL CHECK, and all of ASSEMBLY REPAIR AND REPLACEMENT paragraphs supplied in these manual changes.

Page 8-49, Figure 8-19. A9 Integrator Assy Component Locator/Schematic Diagram:

All Serials	>Change reference designation of resistor marked C24 (top left center) to R24. >Add reference designator R5 to top left unmarked resistor shown below AMP1. >Add reference designator R2 to resistor directly to the right of R5. >Add reference designator R8 to resistor directly below R11.
2632A	>Replace A9 (05065-6015) component locator/schematic diagram with new A9 (05065-6108) component locator/schematic diagram supplied in these manual changes.

Page 8-50, Circuit Diagrams, Theory, and Maintenance:

2120A	Quartz Crystal Oscillator Assembly, A10 Theory: >Replace A10 theory with the new pages 8-50/8-52 supplied in this manual change.

OPERATIONAL AMPLIFIER A9 THEORY

The A9 Assembly amplifies and integrates the output of A8 Phase Detector and provides a dc error signal for controlling the quartz oscillator in A10 Assembly. The front-panel FUNCTION switch provides a means of opening the control loop by shorting the A9 output to its input and placing a large resistance in series with the output.

DC error signals from A8 Phase Detector connect through pin 14 to the input amplifier U3. U3 is a high-impedance, low-noise, precision FET input operation amplifier. It has extremely low input bias current and low input offset voltage. The integrating function is provided by C5 with the integrating time constant being set by the combination of C5 and R5. Initial integrator drift is minimized by zeroing the input offset voltage of U3 using potentiometer R8.

U3 output connects to the A14 Logic Assembly as one logic input and to the CONTROL position of the front-panel CIRCUIT CHECK switch. The front-panel FUNCTION switch does two things:

a. In the OPER position, the output of U3 feeds through R3 to the A10 Quartz Oscillator Assembly and through R1 to the rear-panel CONTROL jack.

b. In the LOOP OPEN position, the output of U3 connects back to the input, disabling the integrator. Additionally, a 100K resistor is placed in series with the U3 output and the A10 Quartz Oscillator Assembly input. This resistance helps isolate the A10 assembly from the A8 Phase Detector Assembly.

A9 MAINTENANCE

NORMAL OPERATION

The integrating amplifier uses the error signal from the phase detector as an input and provides the control voltage for the A10 Quartz Oscillator Assembly. The output voltage swing is limited to ±12 Vdc.

OPERATIONAL CHECK

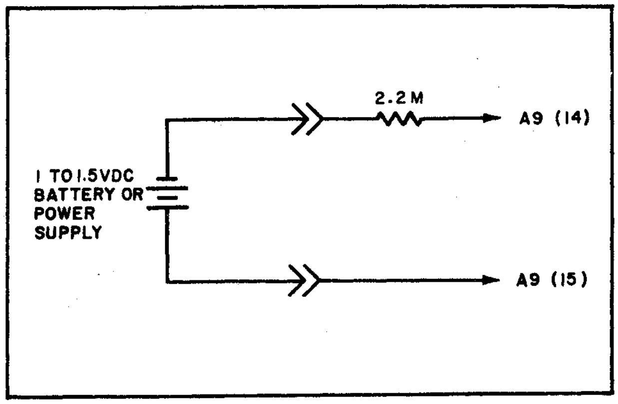
a. Remove A8 circuit board from its socket.

b. Short pins 14 and 15 of A9 Assembly and connect a dc voltmeter to rear-panel CONTROL jack.

c. Set FUNCTION switch to LOOP OPEN and then to OPER. Measure voltage on dc meter. This voltage may be drifting, caused by the integrator circuit integrating the operational amplifier's offset voltage. If voltage drift exceeds 20 mV/minute, A9R8 should be adjusted for minimum drift.

d. Remove short from pins 14 and 15. Set FUNCTION switch to LOOP OPEN and connect circuit as shown:

A9 Test Setup



e. Set dc voltmeter to 30V range. Observing dc voltmeter set HP 5065A's FUNCTION switch to OPER. The voltage will increase at the rate of about 1V/second to about -12V.

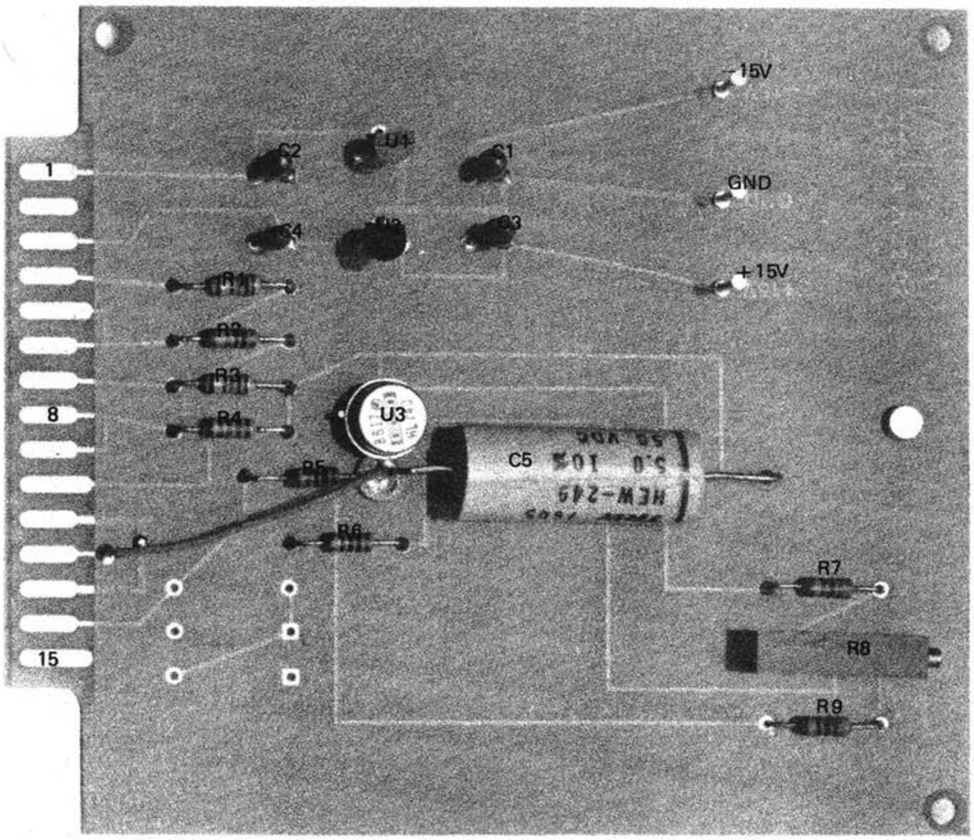
f. Set FUNCTION switch to LOOP OPEN. The voltage will go to ZERO. Now reverse the battery or power supply connections so that the negative terminal is connected to the 2.2 megohm resistor.

g. Set voltmeter to read positive voltages. Set FUNCTION switch to OPER and observe voltmeter reading. Reading should increase at a rate of about 1V per second to a final reading of approximately +12V.

h. Remove connection to A9, pins 14 and 15. Remove dc voltmeter. Reinstall A8 Circuit board. This completes the check.

ASSEMBLY REPAIR AND REPLACEMENT

After repair or replacement of A9 Assembly, A9R8 should be adjusted as described in OPERATIONAL CHECK; steps a, b, and c.



Part of Figure 8-19
A9 INTEGRATOR ASSEMBLY COMPONENT LOCATOR
(05065-6108, SERIES 2632)

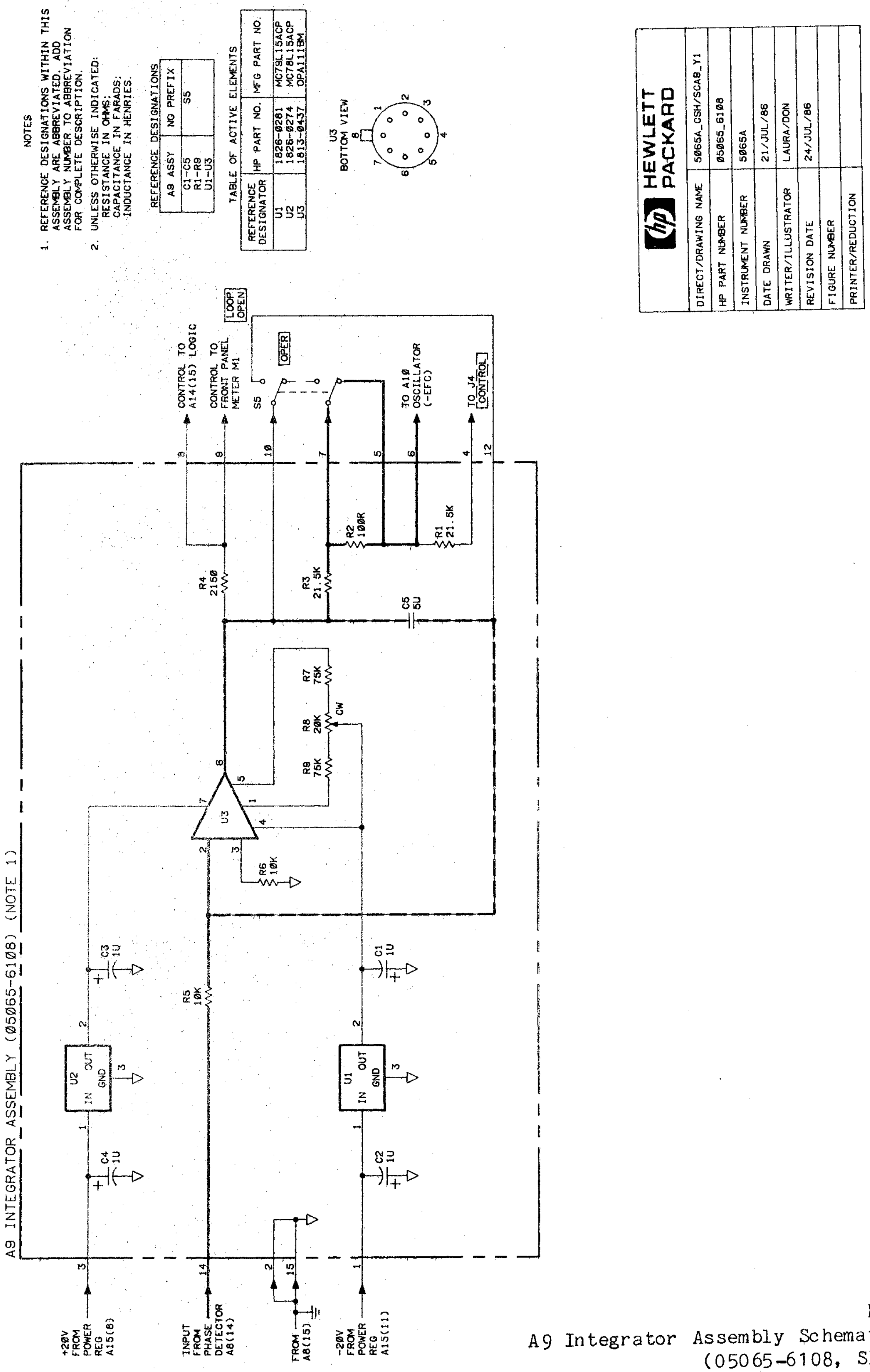


Figure 8-19
A9 Integrator Assembly Schematic Diagram
(05065-6108, SERIES 2632)

QUARTZ CRYSTAL OSCILLATOR ASSEMBLY A10 THEORY

GENERAL THEORY

The A10 Oscillator/Divider Assembly (HP Part No. 05065-6094) provides a stable, high-quality 5 MHz signal at an output level of at least 1 Volt rms into 50 Ohms. This assembly consists of three subassemblies:

1. A10A1 10 MHz Quartz Oscillator Assembly
2. A10A3 Power Supply Assembly
3. A10A2 Frequency Divider/Amplifier Assembly.

A10A2 Frequency Divider/Amplifier divides the 10 MHz to 5 MHz and provides the proper output levels. Electronic Frequency Control (EFC) inputs enable the oscillator frequency to be adjusted electronically as part of a servo loop, or by a potentiometer. The entire A10 assembly is designed to replace the 00105-6013 oscillator formerly used in this instrument.

The A10A1 Quartz Oscillator Assembly (HP Part Number 10811-60109) is covered by the enclosed 10811A/B Operating and Service Manual. Circuit board operation follows:

The 10 MHz output from A10A1 assembly passes through 10 MHz bandpass filter L1 and C5 on A10A3 Power Supply Assembly and then through J1 to edge-triggered D-type flip-flop (A10A2U1) that divides the 10 MHz signal by two. The 5 MHz TTL output at U1(5) passes through 5 MHz bandpass filter L7 and C12. The 5 MHz signal is amplified and filtered by emitter-coupled switch Q1, Q4, and cascade amplifier Q2.

Potentiometer A10A2R8, in the emitter circuit of Q1 and Q4, sets the level at the "5 MHz 1V" output to 1.1 Volts rms into 50 Ohms. The impedance transforming circuit consisting of C8 and L4 allows Q3 to efficiently drive a 50-ohm external load. Choke L3 provides dc to the collector of Q3, C9 blocks dc to the 5 MHz output, and L6 provides a dc return for the external load.

Resistive divider A10A2R5, R4 provides a low-level signal to "5 MHz DIV" output. Nominal voltage at this point is 70 mV rms into 1000 Ohms.

A +15 Vdc reference power supply consists of A10A2CR1, CR2, and associated parts. This supply provides a stable reference source for external circuitry connected to the + or - EFC inputs.

The A10A3 Power Supply Assembly has two inputs; "20V" and "24V". The"24V" input operates from a voltage range of +21 to 30 +Vdc from the HP 5065A. A10U1 regulates this voltage down to +18 Vdc used by oscillator A10A1 oven heater. The +18 Vdc is further regulated to +12 Vdc by A10A3U1 for use in oscillator signal circuits. A10A3CR1, Q1 and associated components regulate the +12 Vdc to +5 Vdc for use by the TTL-divider on A10A2.

Inverting amplifier A10A3Q2 is driven by the "oven monitor" circuit in A10A1 oscillator assembly. It provides an output signal to drive the OSC OVEN meter, or monitor in the HP 5065A.

Electronic frequency control (EFC) signals from the HP 5065A are summed by A10A3R9, R10, R11 and sent to the EFC input of the oscillator assembly. Factory-selected resistor A10A3R11 matches the A10A1 oscillator assembly to the parent HP 5065A. If the A10A3 Power Supply Assembly is replaced, the factory-selected resistor A10A3R11 from the defective board, or a resistor of equivalent value, must be installed in the new board. The value of A10A3R11 must equate the value as noted on the A10A1 oscillator label itself.

A10 MAINTENANCE

GENERAL

A10 Assembly consists of a factory-selected 10 MHz oscillator (HP Part Number 10811-60109) and two circuit board assemblies. A10A2 Assembly divides the A10A1 10 MHz signal by two and provides buffered 5 MHz outputs to both the A3 Multiplier and A6 Frequency Divider assemblies. All input and output connections are on A10A2. The A10A3 is the power supply for the A10A1 and A10A2 assemblies. A10A3 provides an interface between the 5065A power supplies and the circuits in assembly A10.

Input and output connections to A10 are as follows:

CONNECTOR NAME	INPUT OR OUTPUT	SIGNAL CHARACTERISTIC
+24	INPUT	+22 to +30 Vdc primarily for oven heater power (about 160 mA is normal; about 450 mA during warm-up).
+20	INPUT	+18 to +22 Vdc for oscillator and output circuits (50 mA nominal).
+EFC OR -EFC	INPUT	Voltages to control A10 output frequency.
1V	OUTPUT	5 MHz sine wave output. At least 1.0 Vrms into a 50-ohm load.
DIV	OUTPUT	5 MHz sine wave output. Nominal 50 mV to 150 mV rms into 1000-ohm load.
+15	OUTPUT	+14.0 to +15.8 Vdc for fine frequency control (OSC FREQ FINE).
M	OUTPUT	To OSC OVEN position of CIRCUIT CHECK METER via A17 Terminal Board.

OVEN OPERATION

Use the following procedure to check operation of the A10 oven:

a. Apply power to 5065A and allow at least 1 hour warm-up period. Set CIRCUIT CHECK METER to OSC OVEN.

b. Meter indication should be as indicated in *Table 3-1*. Failure of this test indicates failure of A10A1 10 MHz oscillator, or circuit of A10A3Q2.

+15V REFERENCE SUPPLY CHECK

Measure voltage at "+15" jack on A10A2. Voltage should be between +14.0 and +15.8 Volts dc.

OUTPUT AMPLITUDE AND DISTORTION CHECK

Output amplitude at the "1V" jack should be at least 1.0 Volt rms into 50 Ohms. Output harmonics of 5 MHz at the "1V" jack should be at least 30 dB below the 5 MHz output. Output at "DIV" jack should be from 50 mV to 150 mV rms.

a. Disconnect cable at "1V" jack on A10 Oscillator Assembly.

b. Use a Micon-to-BNC test cable and a 50-ohm feedthrough to connect "1V" jack to the vertical input of an oscilloscope. The displayed waveform should be a sine wave of at least 2.8 Volts p-p. This level can be adjusted with A10A2R8.

c. Remove 50-ohm feedthrough and connect signal to spectrum analyzer. Check spectrum from 5 MHz to 20 MHz. All 5 MHz harmonics should be more than 30 dB below the 5 MHz output.

d. Disconnect spectrum analyzer and reconnect 5065A cable on "1V" jack.

e. Use high impedance oscilloscope probe to measure voltage at "DIV" output on circuit side of A10A2 circuit board. Oscilloscope should indicate 140 to 420 mV p-p (50 to 150 mV rms).

SHORT TERM STABILITY CHECK

a. Allow HP 5065A to operate at least one hour. Set FUNCTION to LOOP OPEN.

b. Disconnect cable from A10 "1V" connector and connect cable to an HP 5390A Frequency Stability Analyzer (FSA).

c. Perform short-term stability test of *Table 5-2* (Performance Test, step 8). NOTE: This is a test of the oscillator assembly so the analyzer must be connected to the "1V" output on A10 rather than the 5 MHz front-panel output. All other test conditions remain the same.

The measured stability should be equal to or better than 5×10^{-12} for a one second averaging time. Failure of this test indicates a problem in A10A2 Divider Amplifier Assembly, or A10A1 oscillator. A10A1 may be checked independently.

EFC CHECK

This test checks operation of Electronic Frequency Control (EFC) input to A10.

a. Set CIRCUIT CHECK switch to 2ND HARMONIC and MODE to LOOP OPEN. Turn OSC FREQUENCY FINE control maximum counterclockwise, maximum clockwise, and then back to 250. The CIRCUIT CHECK meter should respond to control movement.

b. Disconnect cable from "-EFC" jack on A10. Connect dc power supply minus (-) lead to "-EFC" jack and power supply (+) to chassis. Slowly adjust power supply from 0 to 5V. CIRCUIT CHECK METER should respond to power supply adjustment. Remove supply and reconnect cable to "-EFC" jack.

A10 REPAIR CONSIDERATIONS

If repair or adjustment of A10 is required, the assembly must be removed from the HP 5065A. Once removed, the A10 assembly can be operated independently by connecting two power supplies. Set one power supply for +22 to +30 Vdc (450 mA maximum current) and connect to the "+24" input. Set the other supply to +20 Vdc (approximately 50 mA) and connect to "+20" input. Power supply (-) terminals are connected to A10 chassis.

An alternate method is to obtain power from the HP 5065A. Using clip leads, connect the A10 chassis to the 5065A chassis. Connect the "+24" terminal on A10 to XA15(4), and the "+20" terminal to XA15(6).

With the A10 removed and operating outside the instrument, troubleshooting is relatively easy. Power supply voltages can be measured on A10A3 sockets. If power supply is defective, remove oscillator assembly A10A1 to gain access to power supply assembly A10A3. A10A3 will operate normally with A10A1 removed.

IF A10A1 IS FOUND TO BE DEFECTIVE, THE ENTIRE A10 ASSEMBLY (05065-6094) MUST BE REPLACED. THE A10A1 10 MHZ OSCILLATOR IS NOT FIELD REPAIRABLE.

The A10A2 (Frequency Divider/Amplifier Board Assembly) and A10A3 (Power Supply Board Assembly) are both repairable to the component level. If the A10A3 is replaced, the factory-selected resistor A10A3R11 from the defective board, or a resistor of equivalent value, must be installed in the new board. The value of A10A3R11 must reflect the value as noted on the A10A1 oscillator itself.

ADJUSTMENTS

There are four adjustments in the A10 assembly: A10A1 output amplitude, frequency, EFC gain, and A10 output level. Assembly A10A1 output amplitude adjustment is covered in the 10811A/B Operating and Service Manual. Frequency adjustment is covered as part of the 5065A operating procedure. A10 output amplitude and EFC gain adjustments are covered below.

OUTPUT AMPLITUDE ADJUSTMENT

a. With A10 operating outside the 5065A as previously described, connect A10 "1V" output through a 50-ohm feedthrough to an oscilloscope vertical input.

b. Adjust A10A3R8 for an oscilloscope display of 3.1 Volts p-p (1.1 Volts rms).

c. Remove connections to A10 and replace in HP 5065A.

A10 ASSEMBLY REPLACEMENT

The HP 5065A does not require internal adjustments following replacement of oscillator assembly A10. After installation is completed, follow the turn-on procedure in *Figure 3-2* of the Operating and Service Manual.

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 8-53, Figure 8-20. A10 Oscillator Assembly Block Diagram:

2120A	>Replace A10 block diagram with A10 schematic diagram supplied in these manual changes.
2142A	>Change A10 (05065-6094) SERIES to 2134. >Change A10, A10A3 component locator SERIES to 2134. >Change A10A3R12, R13 value to 464 ohms.
2432A	>Change A10A2 p/n from 05061-6165 to 05061-6174, SERIES 2432. >Change A10A2R11 value to 147K. >Replace A10A2 (05061-6165) component locator with new A10A2 (05061-6174) component locator, SERIES 2432 supplied in these manual changes.
2644A01507 and above	>Replace A10A2 (05061-6174) schematic diagram with new A10A2 schematic diagram (05061-6199, SERIES 2736A. >Change A10A2R1 value from 464 ohms to 383 ohms.

Page 8-55, Figure 8-21. A11 RVFR Temperature Controller Assembly:

All Serials	>Replace A11 component locator with new A11 component locator supplied in these manual changes.

Page 8-63, Figure 8-23. A14 Logic Assembly:

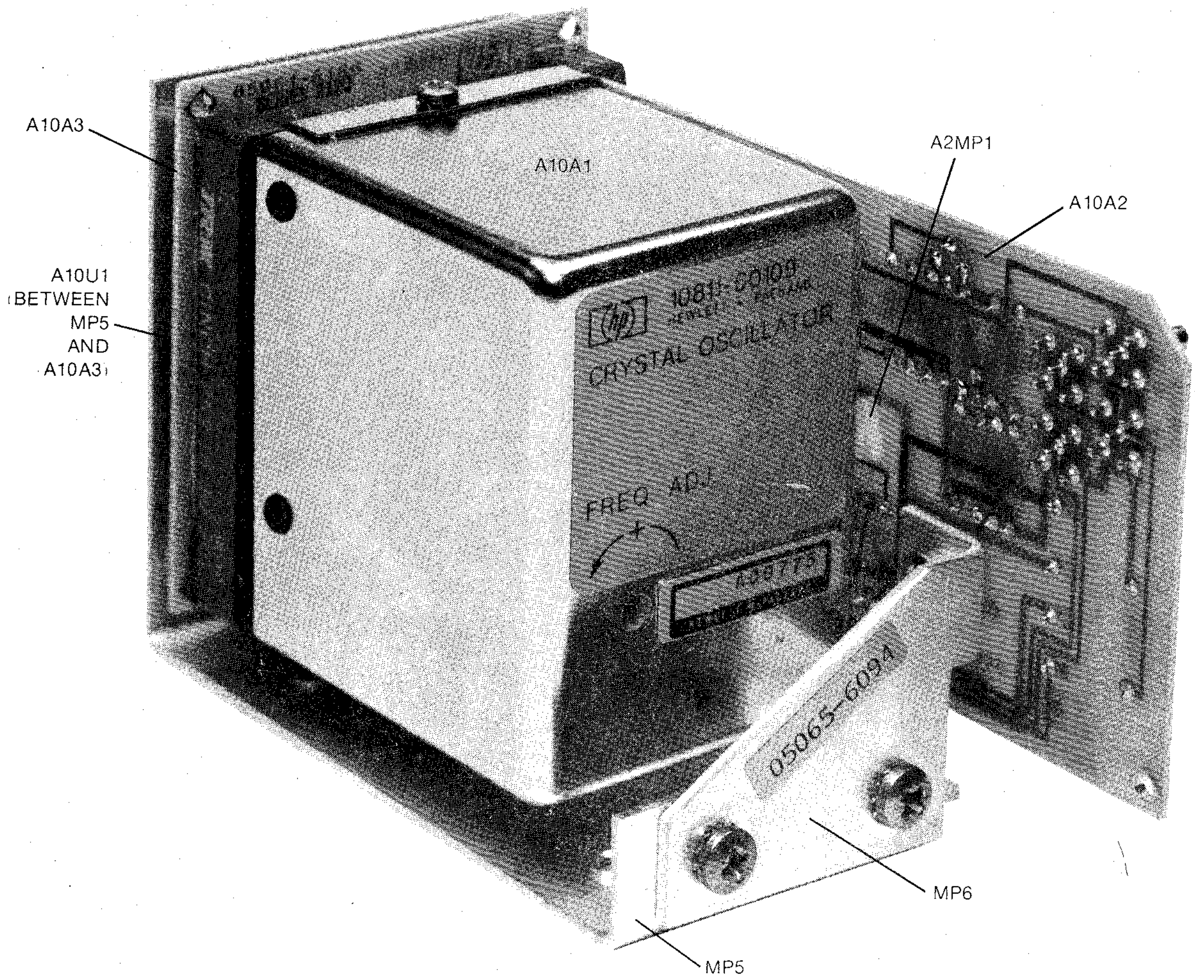
All Serials	>Change the value of R12 (20K) to 1000 ohms. >Add R15 (20K) between circuit board common and junction of CR2 and R16.

Page 8-64. Circuit Diagrams, Theory, and Maintenance:

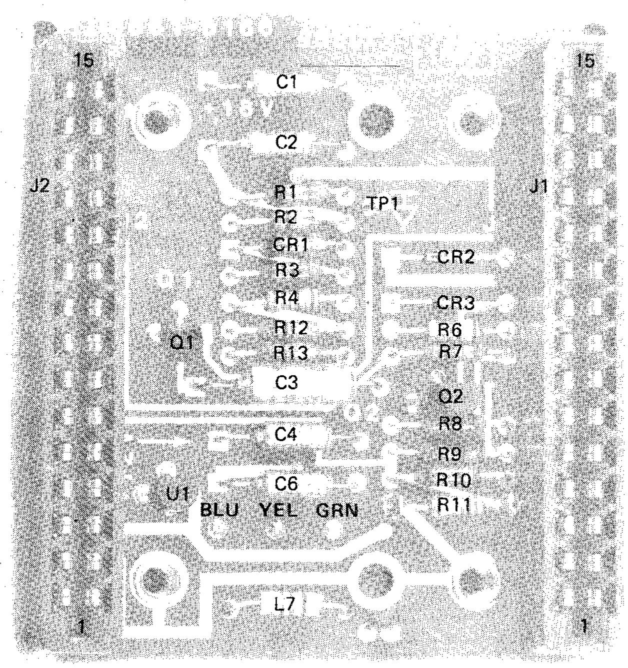
2144A	Power Supply and Regulator Circuit A15 Theory: >Add the following to paragraph a: "Starting with the A15 (Part No. 05065-610, SERIES 2144) the bridge rectifier diodes on A15 are replaced by chassis-mounted bridge rectifier CR4."

Page 8-65, Figure 8-24. A15 Power Supply and Regulator Assembly:

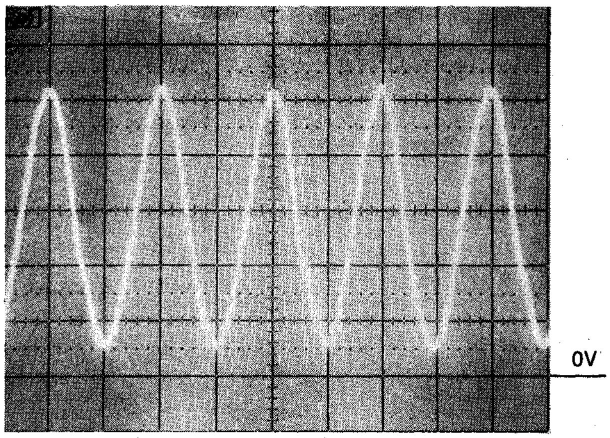
All Serials	>Change part number of Q7 from 1853-0006 to 1853-0012. >Add reference designation (C12) to disc capacitor loaded directly below resistor R14, in A15 component locator.
2144A	>Change A15 p/n from 05065-6023 to 05065-6100, SERIES 2144. >Delete all connections to A15 terminals 12, 13, 14, and 15. >Delete C1 and diodes CR1-CR4 in component locator and schematic diagram. >Add a connection by a wht-brn-yel wire (CR4 +) to the junction of C7 and L1 and mark the wire "+24V-32V FROM



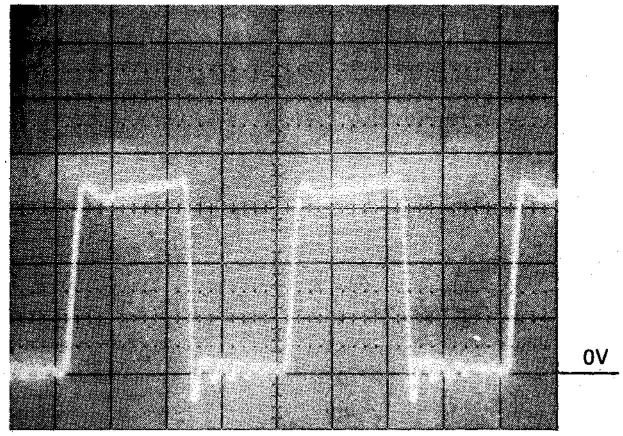
A10 OSCILLATOR ASSEMBLY (05065-6094 SERIES 2120)



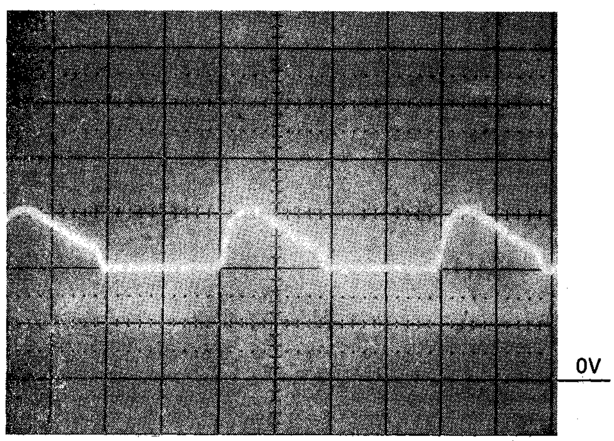
A10A3 POWER SUPPLY ASSEMBLY (05061-6166 SERIES 2120)



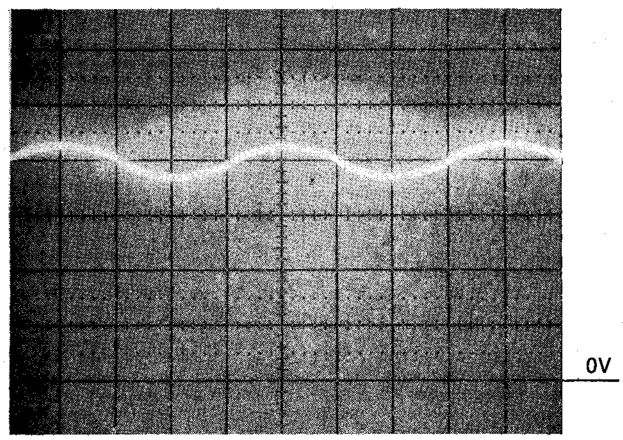
(1) **Vert** = .5V/div.
Horiz = 50 ns/div.



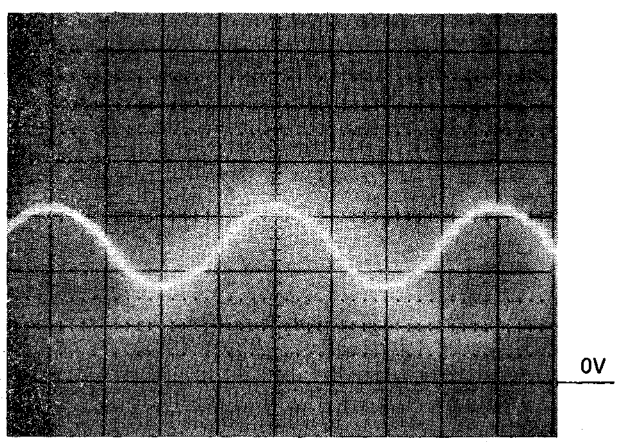
(2) **Vert** = 1V/div.
Horiz = 50 ns/div.



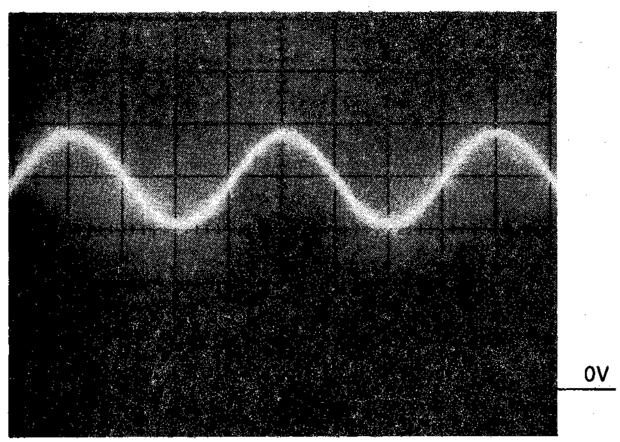
(3) **Vert** = 2V/div.
Horiz = 50 ns/div.



(4) **Vert** = 5V/div.
Horiz = 50 ns/div.

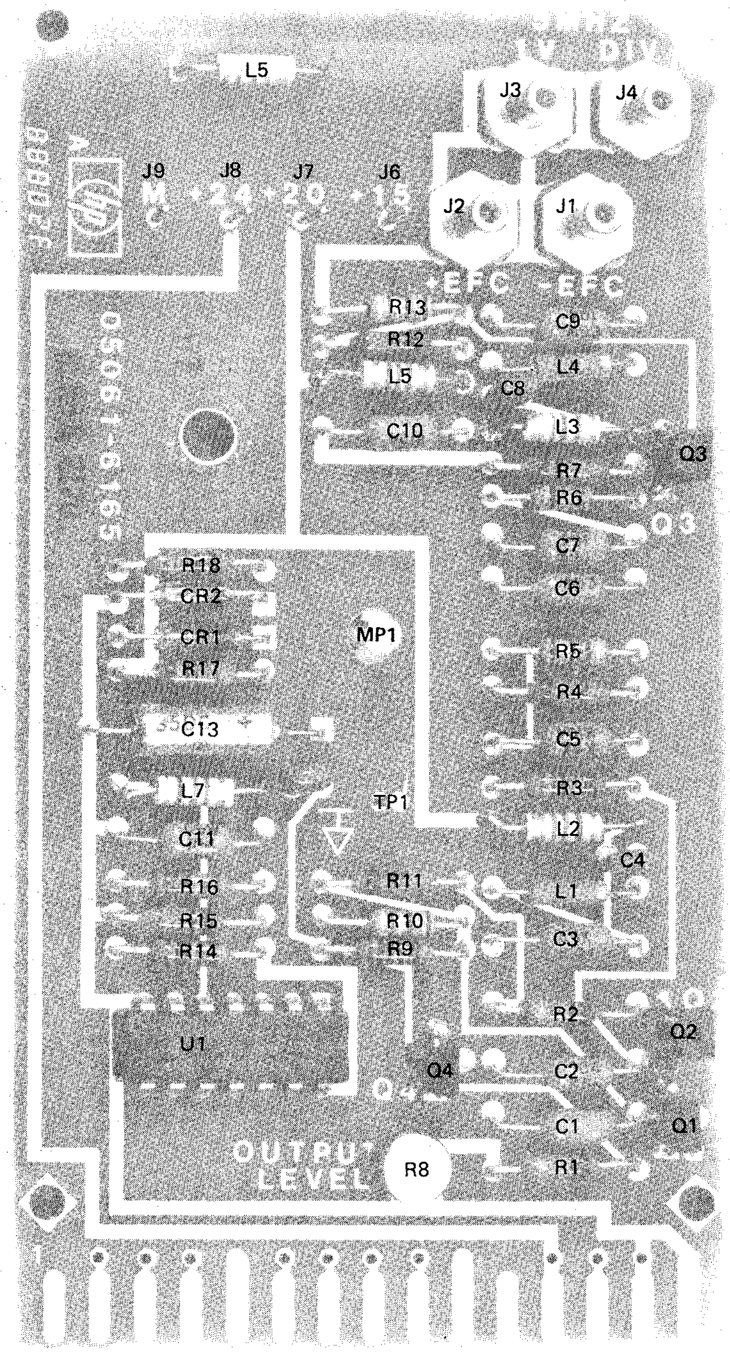


(5) **Vert** = 2V/div.
Horiz = 50 ns/div.

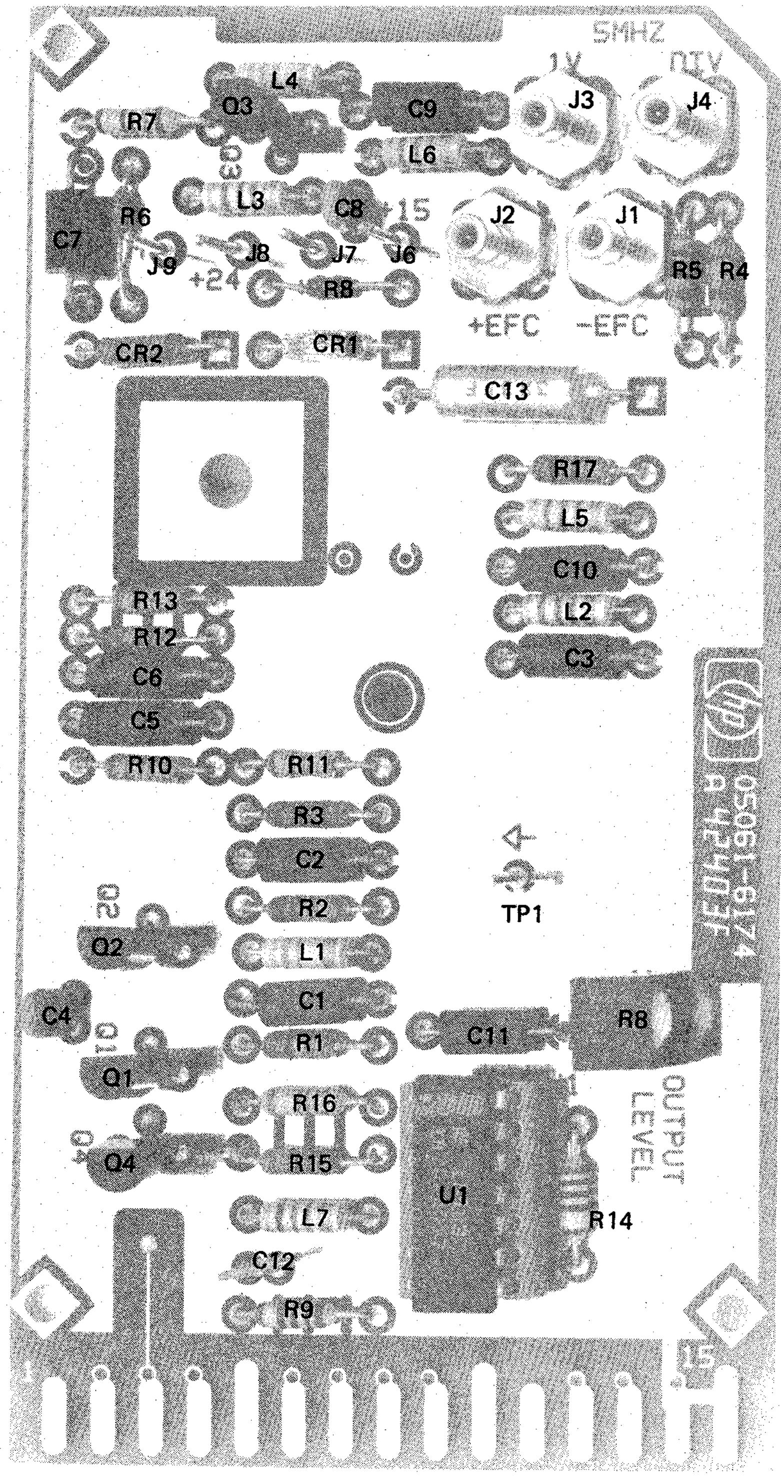


(6) **Vert** = 5V/div.
Horiz = 50 ns/div.

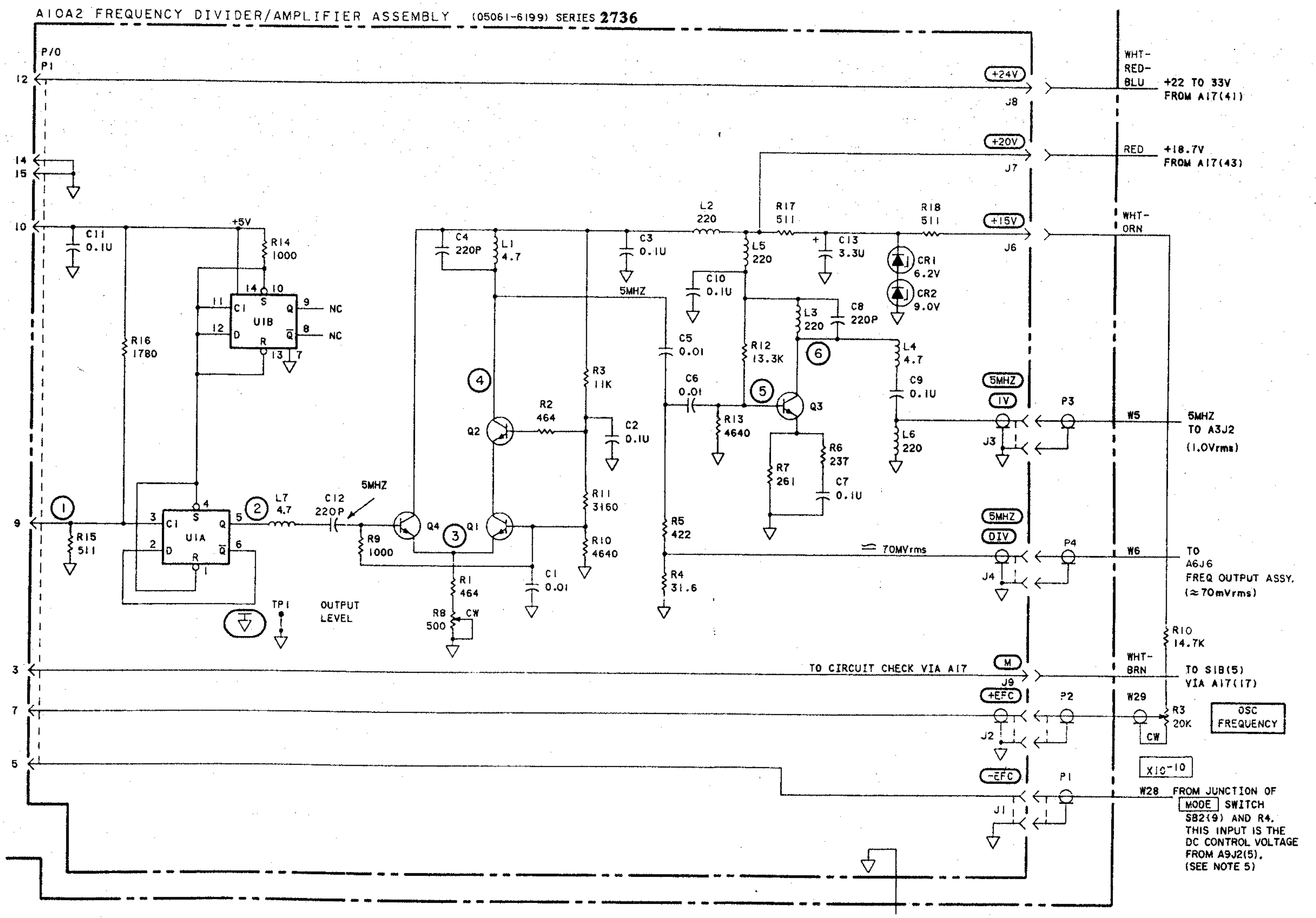
WAVEFORMS FOR A10A2 FREQUENCY DIVIDER/AMPLIFIER ASSEMBLY
(05061-6165 SERIES 2120)



A10A2 FREQUENCY DIVIDER/AMPLIFIER ASSEMBLY
(05061-6165 SERIES 2120)



A10A2 Frequency Divider/Amplifier Assembly
Component Locator
(05061-6174 SERIES 2432)



NOTES:

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED, ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN MICROHENRIES.
3. * INDICATES FACTORY SELECTED VALUE.
4. CHASSIS CONNECTION MADE BY A10A2 MOUNTING SCREW.
5. DC CONTROL VOLTAGE CAN RANGE BETWEEN -5Vdc AND +5Vdc, DEPENDING ON THE FREQUENCY DIFFERENCE BETWEEN THE CESIUM RESONANCE AND THE APPLIED MICROWAVE SIGNAL SYNTHESIZED FROM THE A10A1 10MHz OUTPUT. "ALARM" LED IS SET TO TURN ON AT >+4.5Vdc (NOMINAL) AND < -4.5Vdc (NOMINAL).

REFERENCE DESIGNATIONS

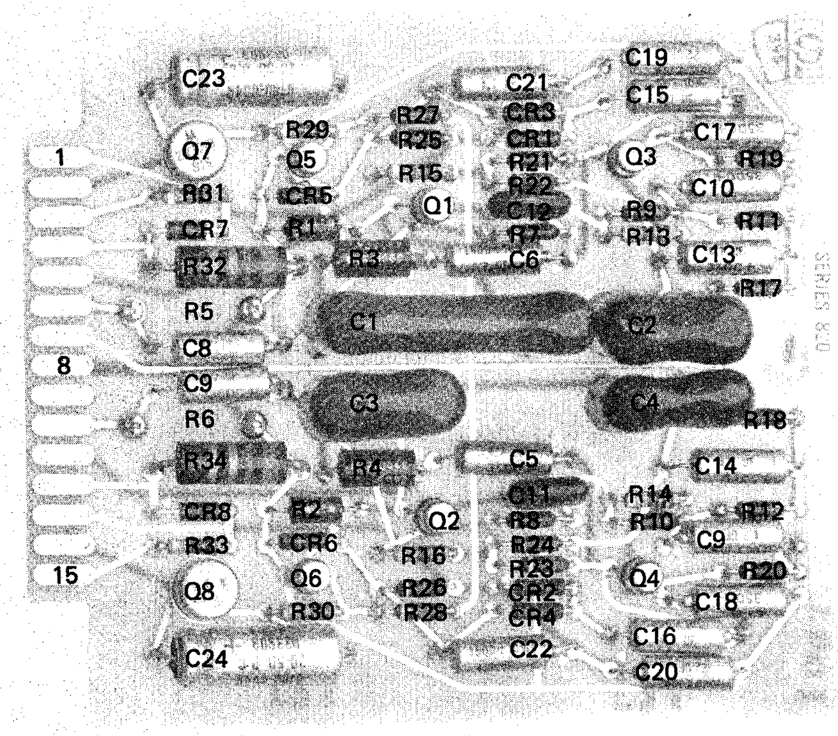
NO PREFIX	A10A1	A10A2	A10A3
R10		C1-13 CR1,2 J1-4,6-9 L1-7 Q1-4 R1-18 TP1 U1	C1-7 CR1-3 J1,2 L1 Q1,2 R1-4,6-13 TP1 U1

NOT ASSIGNED: A10A2J5, A10A3R5

TABLE OF ACTIVE ELEMENTS

CIRCUIT REF.	HP AND MFR PART NO.
A10U1	1826-0390 (LM317T)
A10A2CR1	1902-0033 (1N823)
A10A2CR2	1902-0787 (1N938)
A10A2Q1-Q4	1854-0215 (2N3904)
A10A2U1	1820-0077 (SN7474N)
A10A3CR1	1902-0984
A10A3CR2,CR3	1901-0050
A10A3Q1	1854-0831 (2N6429A)
A10A3Q2	1854-0215 (2N3904)
NOTE--ALL TRANSISTORS ARE NPN SILICON	

Part of Figure 8-20
A10A2 Frequency Divider/Amplifier Assembly
Schematic Diagram
(05061-6199, SERIES 2736)



Part of Figure 8-21. A11 RVFR Temperature Controller Assembly
(05065-6024, SERIES 1840)

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 8-66. Circuit Diagrams, Theory, and Maintenance:

All Serials

DIGITAL DIVIDER POWER SUPPLY A16 THEORY

>Change first line to read, "The A16 module has two basic circuits".

>Delete paragraph "c".

>Change second sentence in first paragraph at top of column to: "In T2 output, CR10 provides isolation."

>Replace second paragraph in column two with the following: "The 1 PPS pulses from A5 Digital Divider output connector (J1) are input as MASTER 1 PPS pulses at terminal W on Clock Display Assembly A19."

>Delete third paragraph under "A16 MAINTENANCE".

Page 8-67, Figure 8-25. Figure 8-25. A16 Digital Divider Power Supply Assembly:

All Serials

>Change reference designation of diode CR13 to CR12, located between R19 and R20 (upper left corner).

>Change reference designation of diode directly to the left of R10 (top center) from R15 to CR10.

>Add resistor R15 betweeen the two terminal posts just above R17.

Reference Designator Table

>Change CR1-15 to CR1-12,15.

>Change Q1-12 to Q1-10.

>Change R1-26 to R1-20.

2148A

>Change A16,A16A1 SERIES to 2148.

>Add to NOTES:

4. Transistor 1854-0916 is a preferred part. A16 and A16A1 SERIES 2148, which use the 1854-0916 transistor for Q9, Q10, are directly interchangeable with prior series. These assemblies are used in Opt 001 and 003 only. Option series changes do not affect the serial prefix in this instrument.

Table of Active Components

>Change Q9, Q10 to 1854-0916.

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 8-71, Figure 8-26. A19 Clock Display Assembly:

All Serials	>Change part numbers at top of A19A2 schematic to (05061-6125 for OPTION 001) and (05061-6136 for OPTION 003). >Delete connection between collector of A19A1Q3 and A19A1U2 pins 11 and 14. >Connect A19A1U2 pins 11 and 14 to board common.